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MS-7733 Ver: 3.0 Mini ITX

Intel -MahoBay plamform

CPU:

INTEL-Ivy bridge LGA1155

System Chipset:

INTEL-Panther Point

OnBoard Chipset:

HD Audio Codec:RTL887
LAN-RTL8111E Co-lay 8105E
SIO:Fintek F171808A
Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

SO-DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PWM:

VRD12 - UT501+3Phase

ACPI:

UPI

Other:

SATA(SATA2-300MB/s*3 + SATA3-500MB/s *1)
Rear USB2.0 *4+ Front USB2.0*4
REAL USB3.0 *2
FRONT USB3.0 *2

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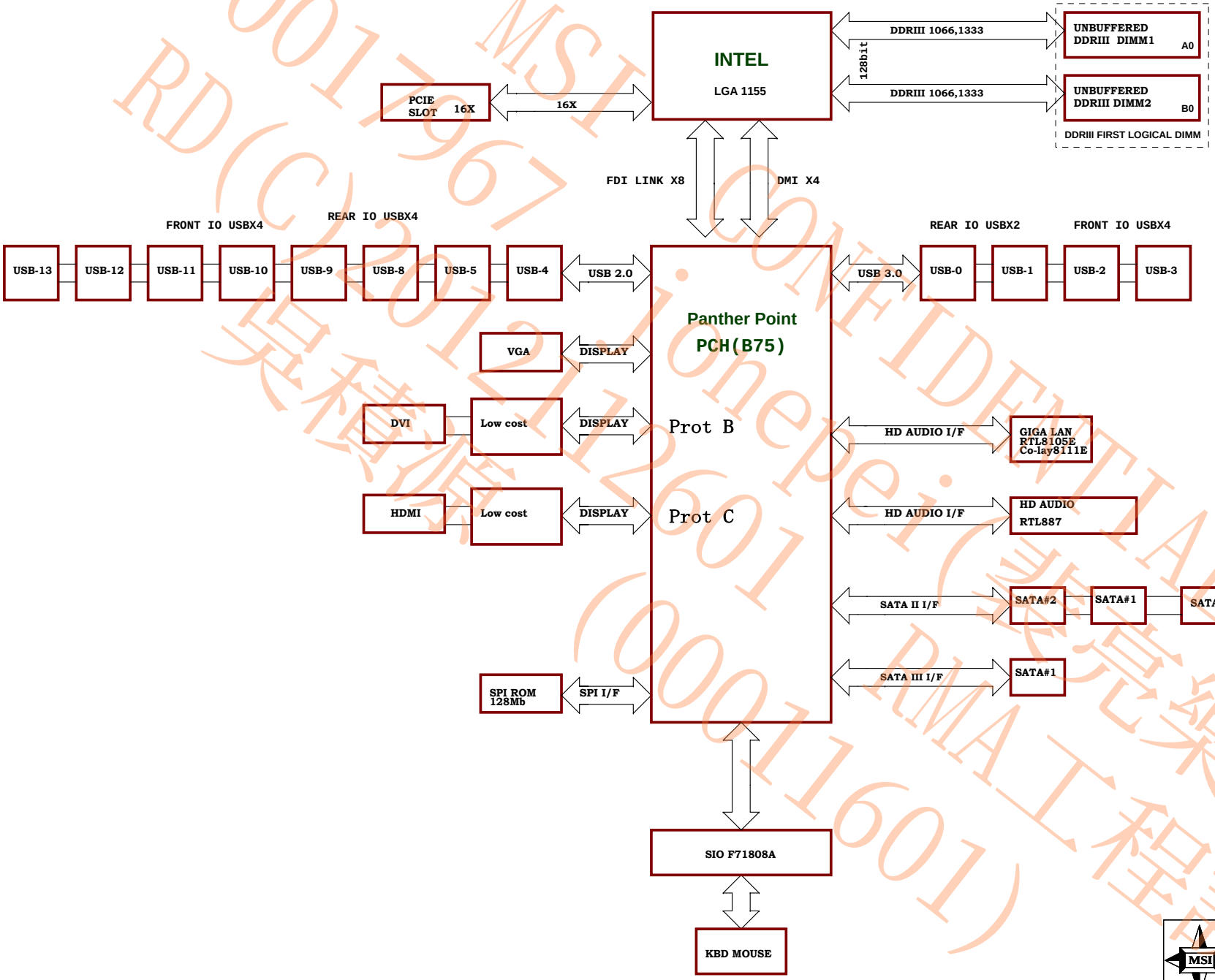

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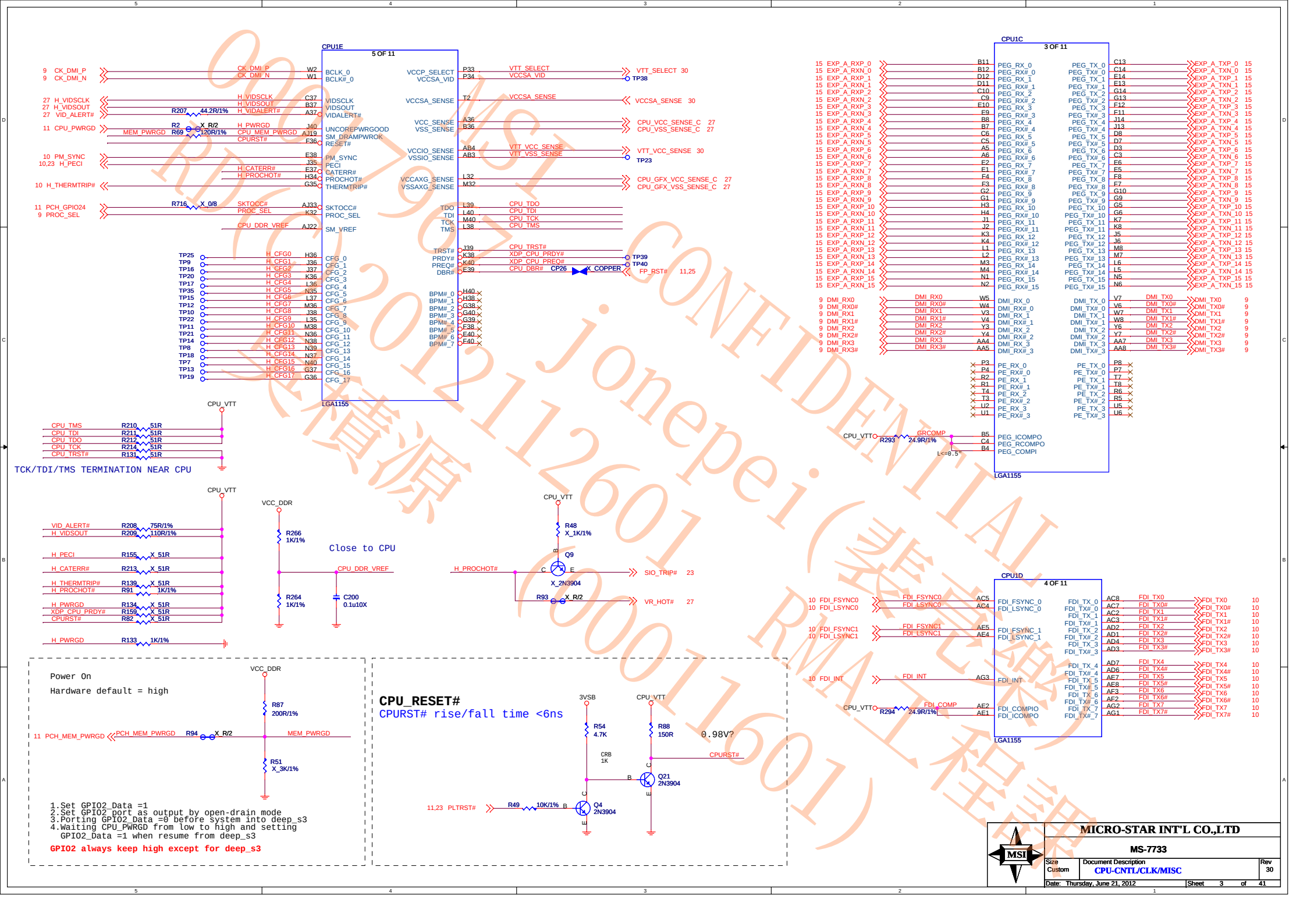
CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
TCK/TDI/TMS TERMINATION NEAR CPU
Close to CPU
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2_port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
CPURST# rise/fall time <6ns
0.98V?
MICRO-STAR INT'L CO.,LTD
MS-7733
Size Custom
Document Description CPU-CNTL/CLK/MISC
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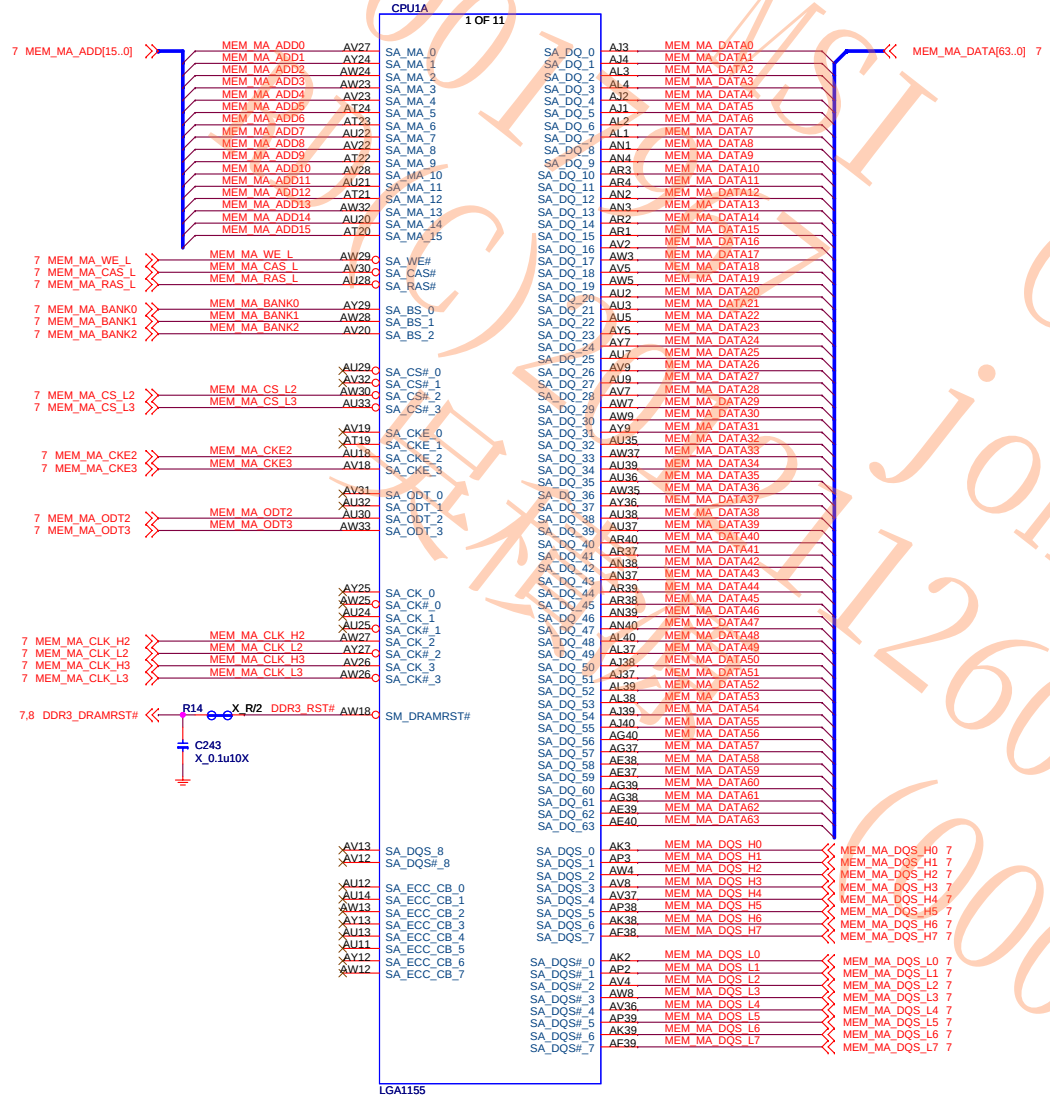

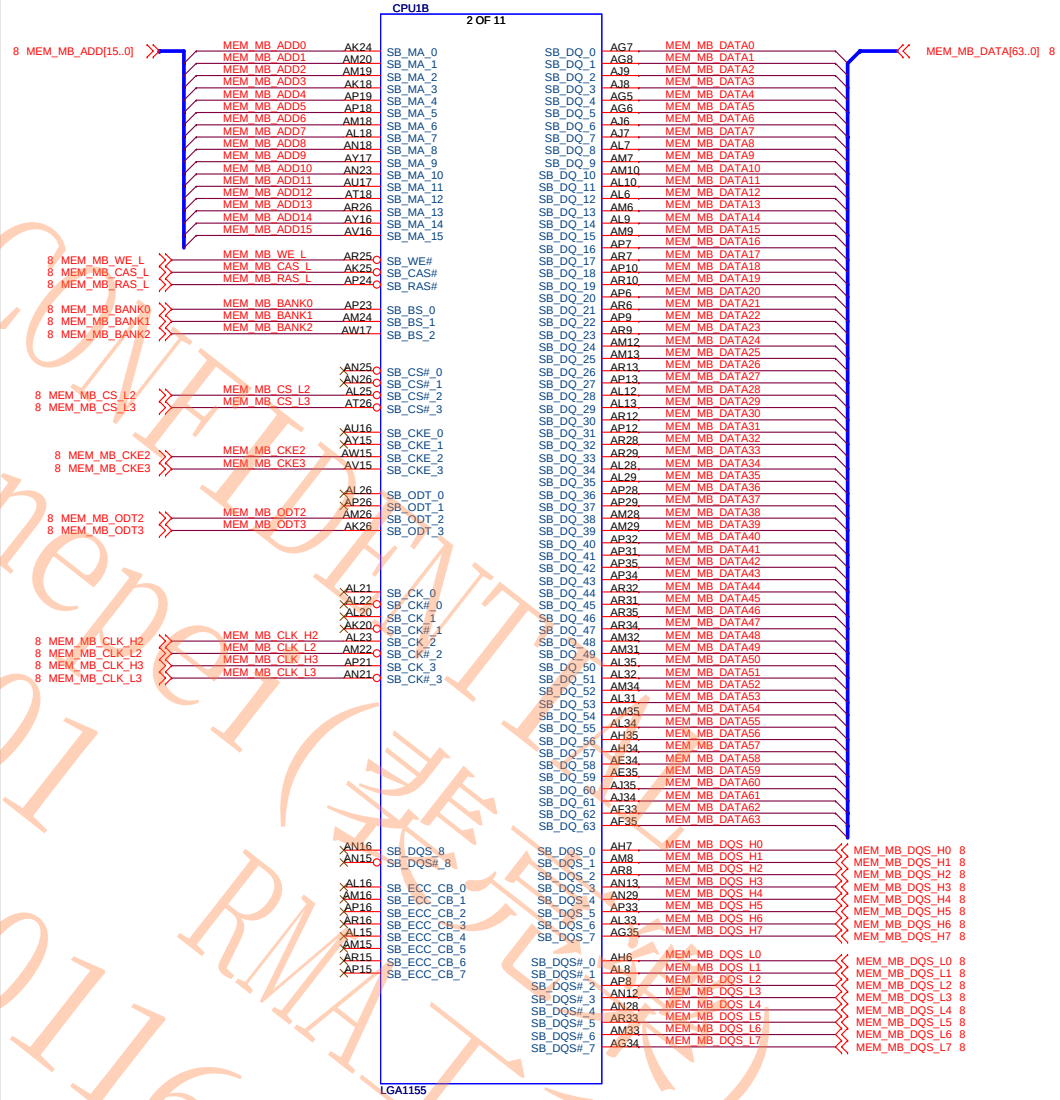

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2012601 RMA工程師
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Size	Document Description	Rev
Custom	CPU-Memory	30

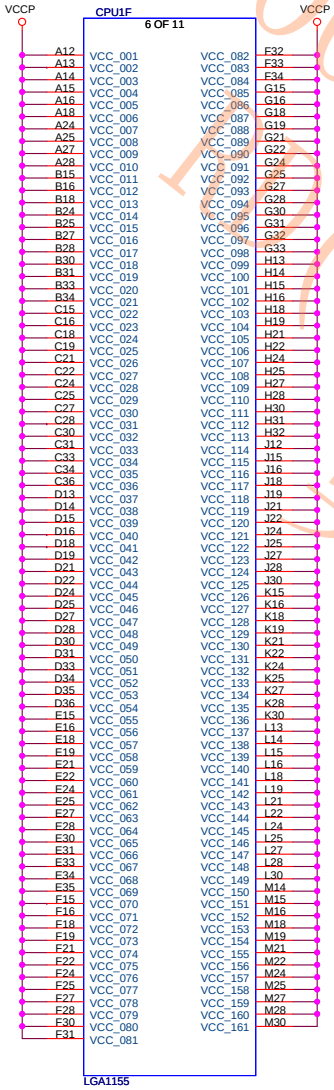
Date: Thursday, June 21, 2012 Sheet 4 of 41

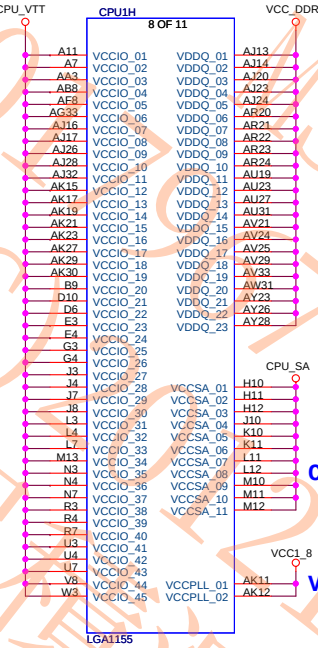
VCCP: 112A

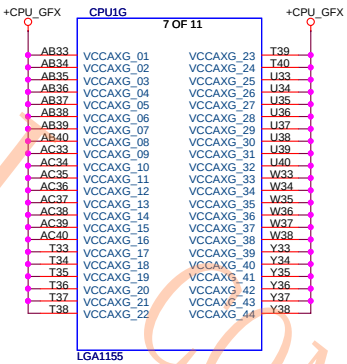
1.05V
CPU_VTT: 8.5A

OC MAX: 1.8 V
VCC_DDR: 4.5A

+CPU_GFX:35A







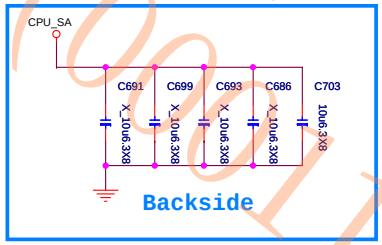
CPU_SA

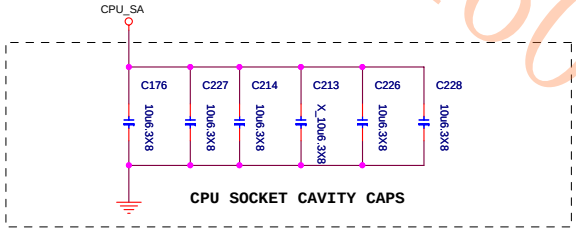
(0.925V / 0.85V)

CPU_SA: 8.8A

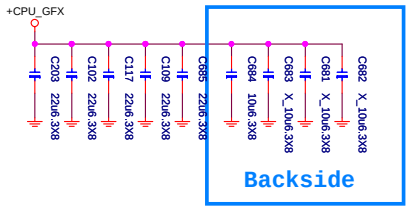
VCC1_8

VCC1_8: 1A



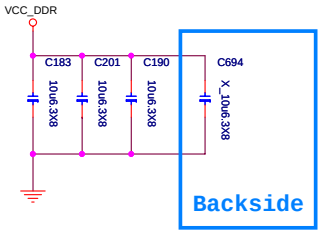


+CPU_GFX Decoupling

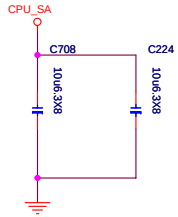


CPU SOCKET CAVITY CAPS

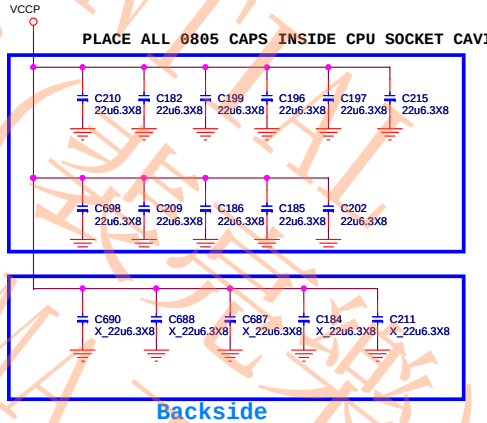
+1.5V_DDR3-Decoupling

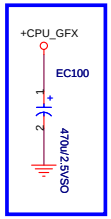


CPU SOCKET CAVITY CAPS



+CPU_VCCP-Decoupling





Bottom side

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Date: Thursday, June 21, 2012	Sheet 5 of 41	

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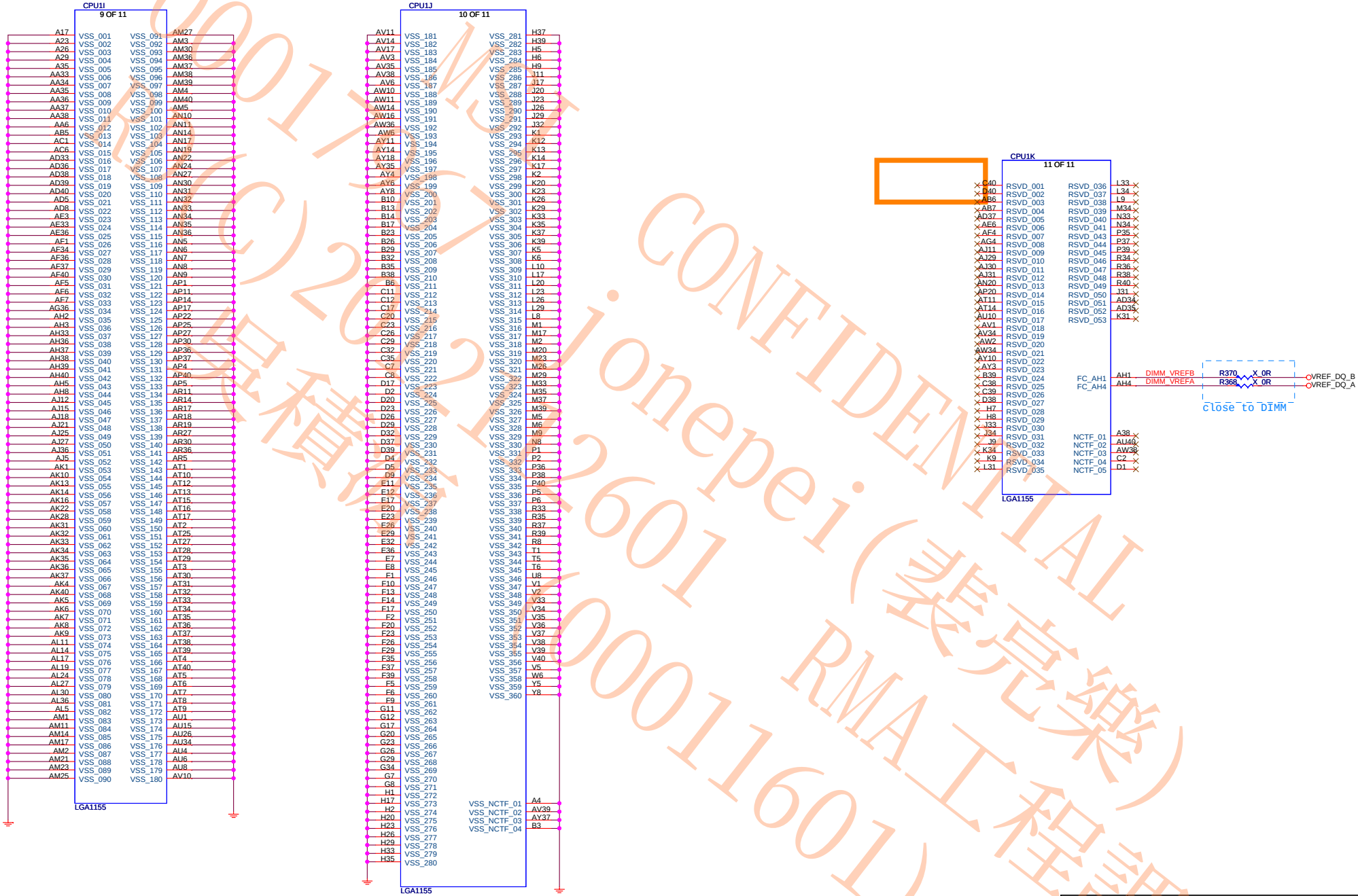
P211260 (0801601)



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MS-7733

Size	Document Description	Rev
Custom	CPU-GND	0A

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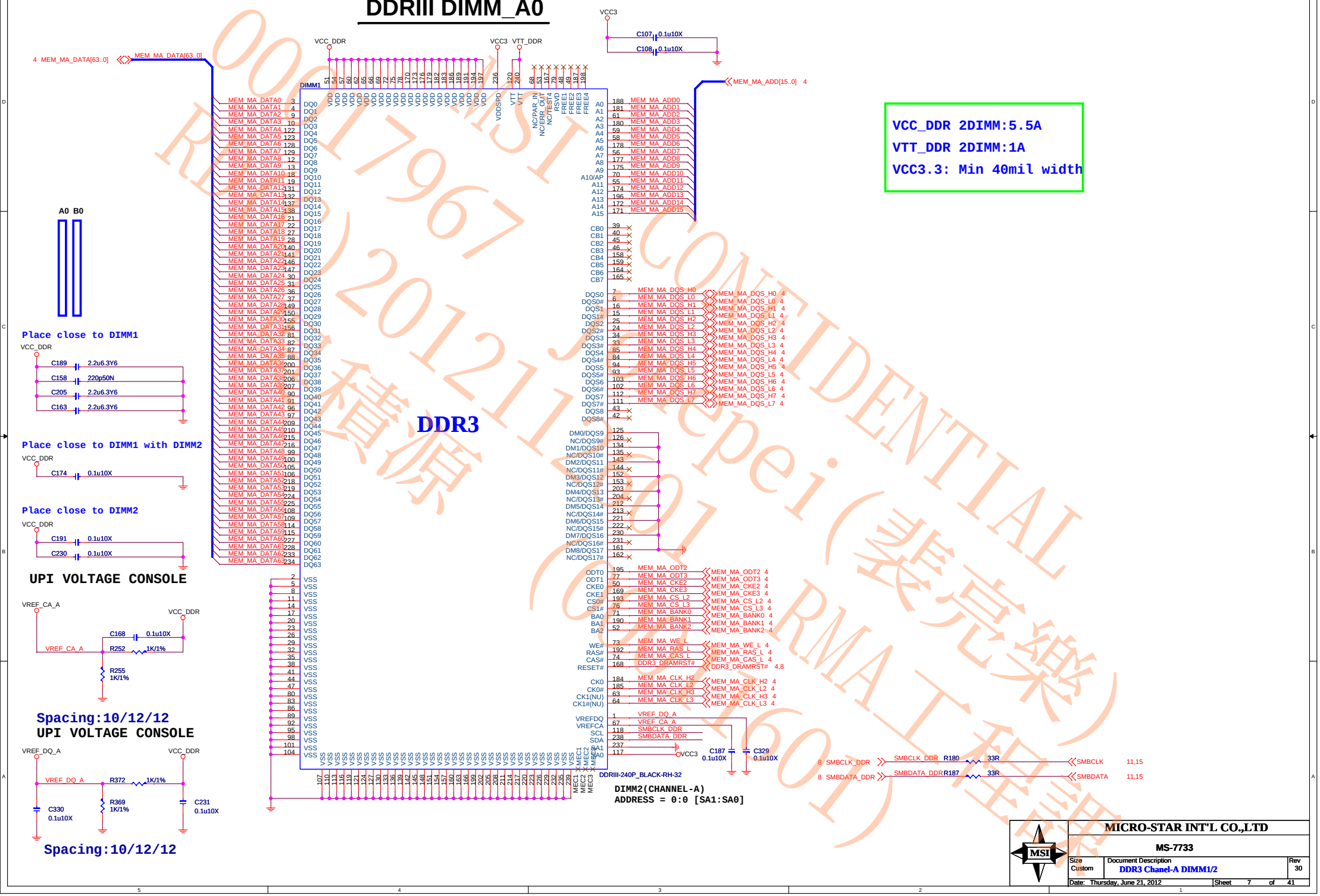
DDRIII DIMM_A0



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MS-7733	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2 — Rev: 30
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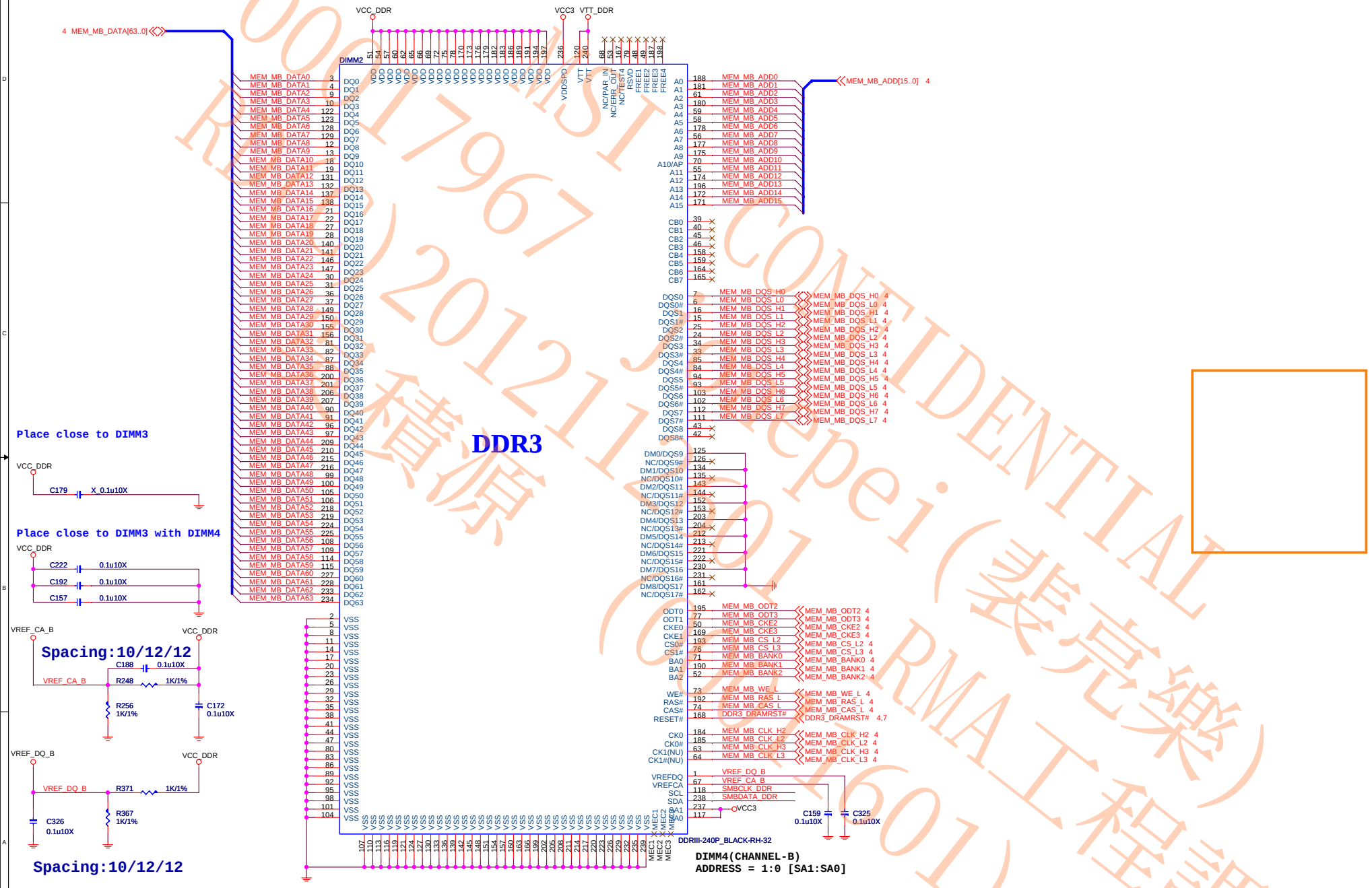
DDRIII DIMM_B0



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RE(C)2012112601
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Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4	Rev: 30
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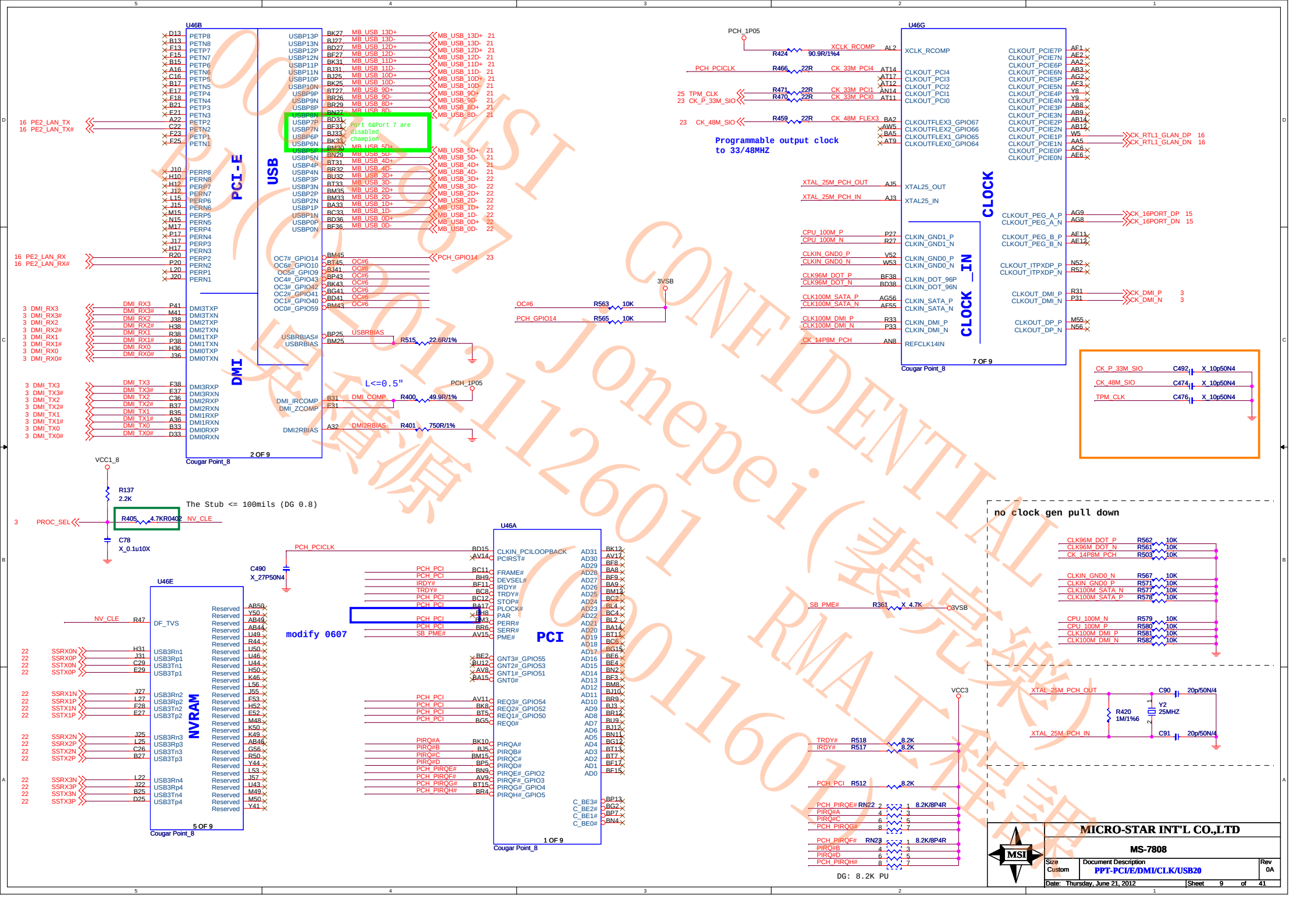
U46B
PCI-E
USB
DMI
Cougar Point_8
2 OF 9
Port 6&Port 7 are disabled champion
U46G
CLOCK
CLOCK_IN
7 OF 9
Programmable output clock to 33/48MHZ
U46E
NVRAM
5 OF 9
modify 0607
U46A
PCI
1 OF 9
The Stub <= 100mils (DG 0.8)
L<=0.5"
no clock gen pull down
DG: 8.2K PU
MICRO-STAR INT'L CO.,LTD
MS-7808
Size Custom
Document Description PPT-PCI/E/DMI/CLK/USB20
Rev 0A
Date: Thursday, June 21, 2012
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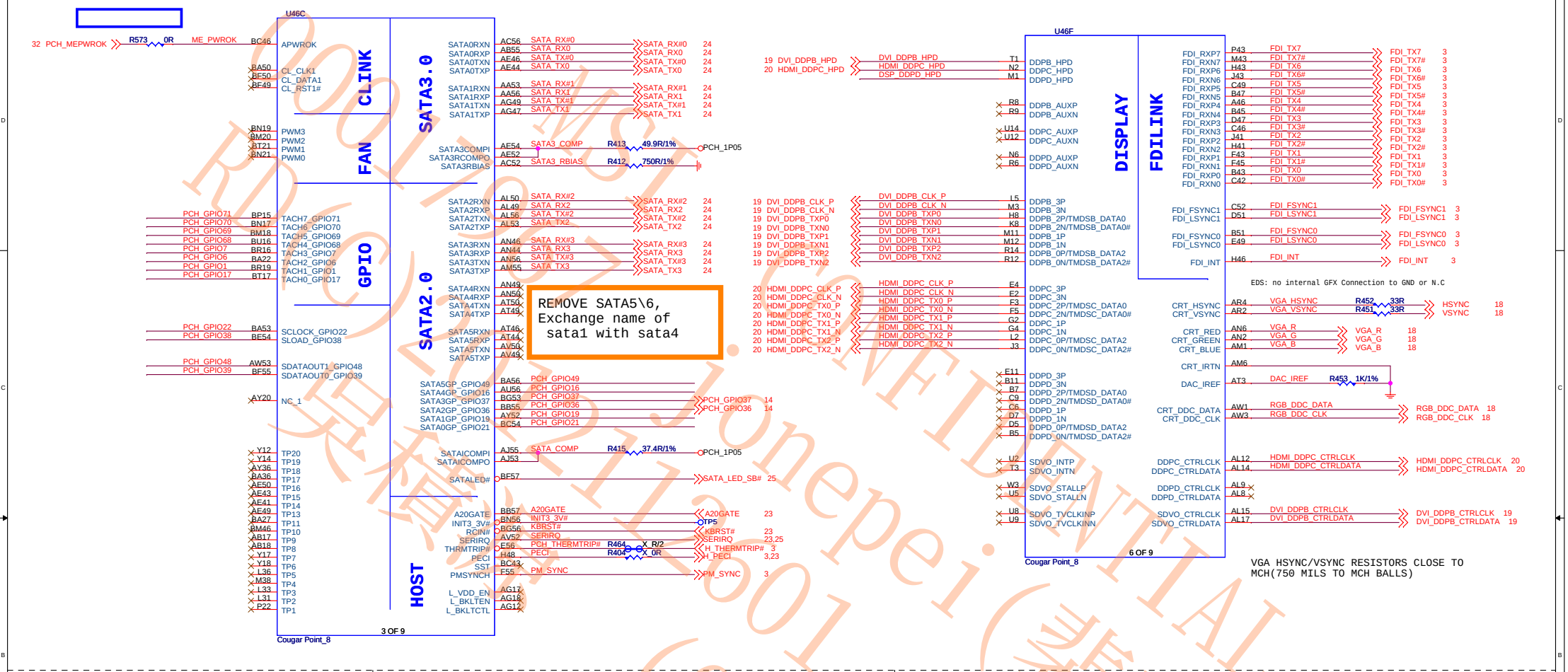
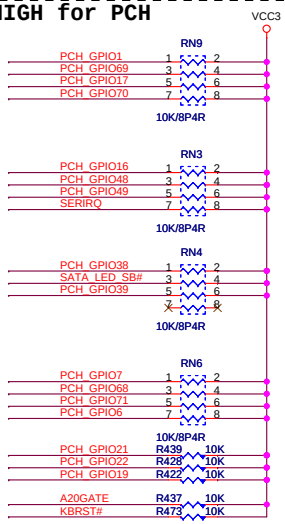


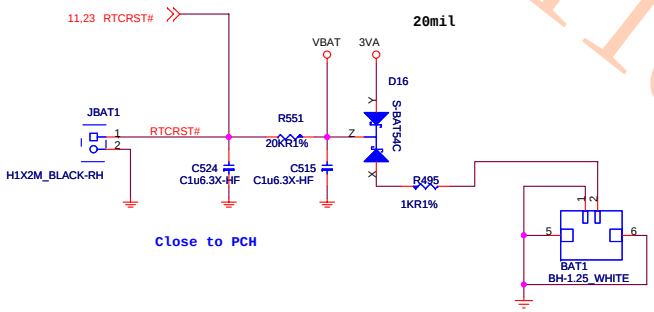
Pull HIGH for PCH



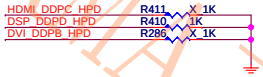
RTC and CLR_CMOS

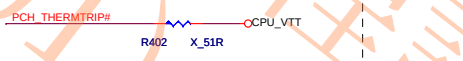
Clear CMOS

CMOS CLEAR JUMPER	
JBAT1 Clear CMOS	
1 - 2	Clear CMOS

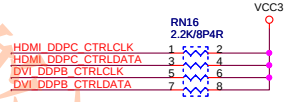


No Display port(pull down)





Enable VGA(CTRLCLK/DATA Pull High)



Close to PCH within 250 mils.

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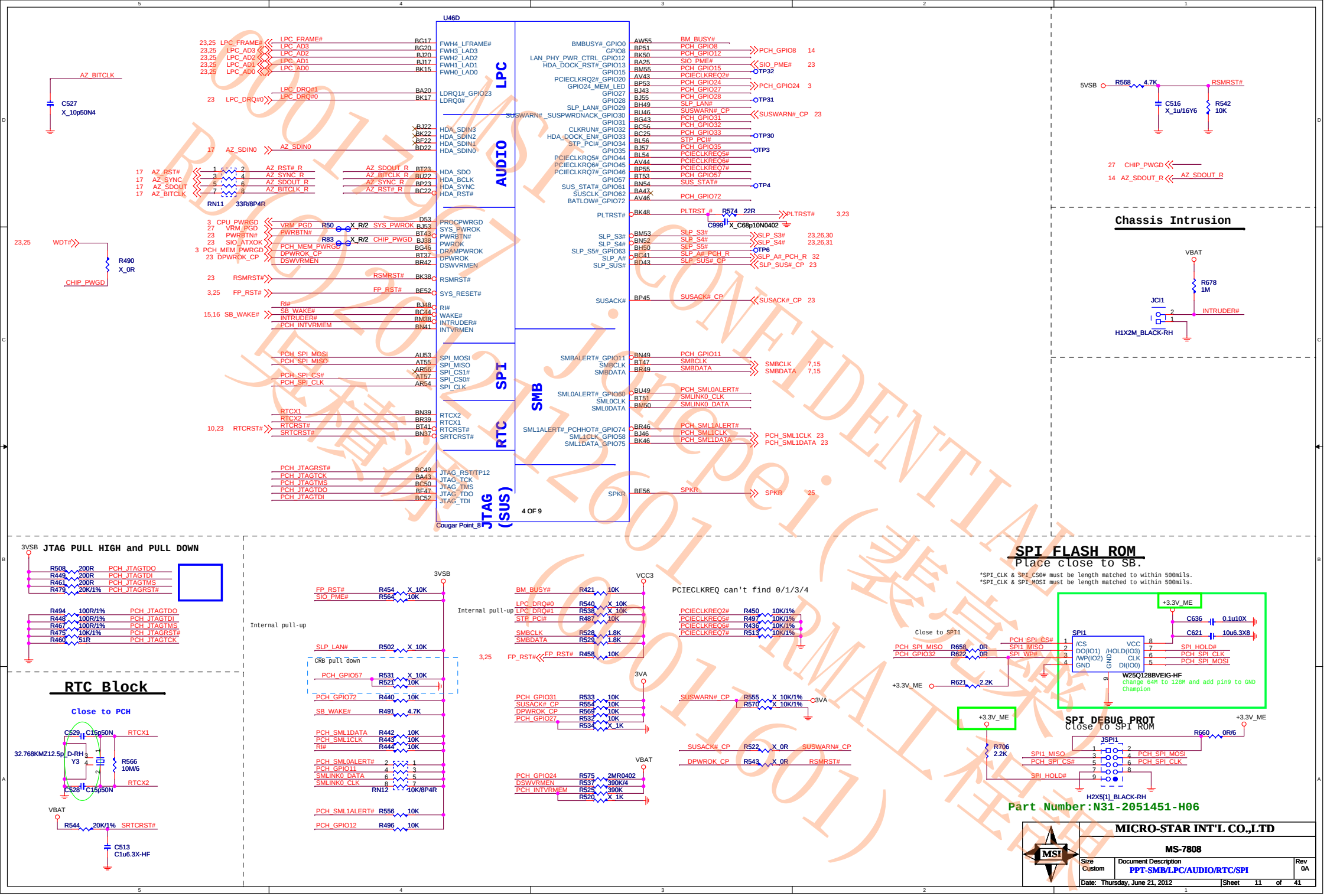
001/09/27 Wistron NEIHU TAI
RMA工程部 (0001601) 程煒(蕭光樂)


U46D
LPC
AUDIO
SPI
RTC
JTAG (SUS)
SMB
4 OF 9
Cougar Point_8
Chassis Intrusion
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
SPI FLASH ROM
Place close to SB.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
W25Q128BVEIG-HF
change 64M to 128M and add pin9 to GND
Champion
SPI DEBUG PROT
Close to SPI ROM
H2X5[1]_BLACK-RH
Part Number:N31-2051451-H06
PCIECLKREQ can't find 0/1/3/4
Internal pull-up
CRB pull down
MICRO-STAR INT'L CO.,LTD
MS-7808
Size Custom
Document Description
PPT-SMB/LPC/AUDIO/RTC/SPI
Rev 0A
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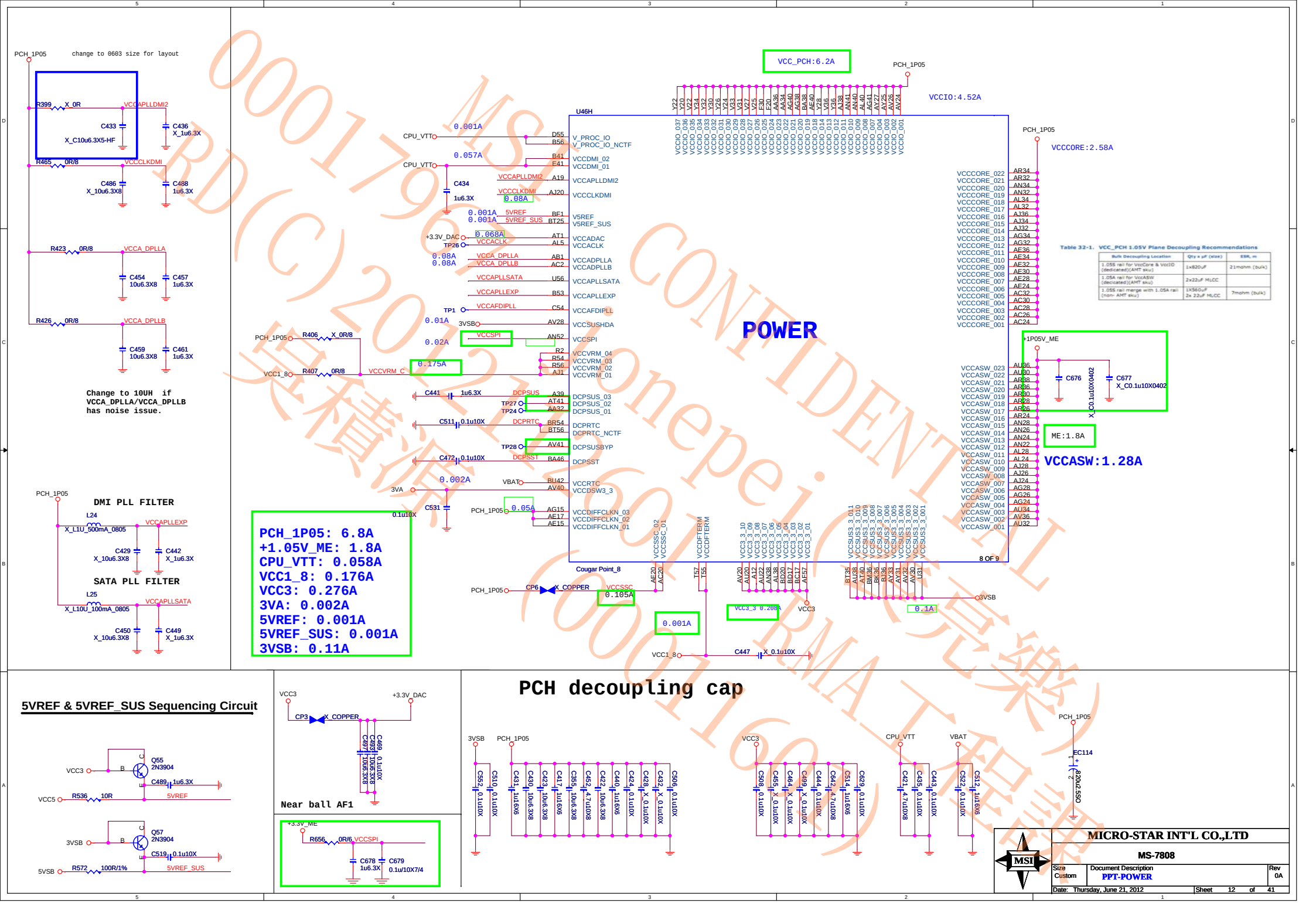
POWER
U46H
VCC_PCH:6.2A
VCCIO:4.52A
VCCCORE:2.58A
VCCASW:1.28A
ME:1.8A
PCH_1P05: 6.8A
+1.05V_ME: 1.8A
CPU_VTT: 0.058A
VCC1_8: 0.176A
VCC3: 0.276A
3VA: 0.002A
5VREF: 0.001A
5VREF_SUS: 0.001A
3VSB: 0.11A
Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
DMI PLL FILTER
SATA PLL FILTER
5VREF & 5VREF_SUS Sequencing Circuit
PCH decoupling cap
Near ball AF1
Cougar Point_8
8 OF 9
MICRO-STAR INT'L CO.,LTD
MS-7808
PPT-POWER
Size Custom
Rev 0A
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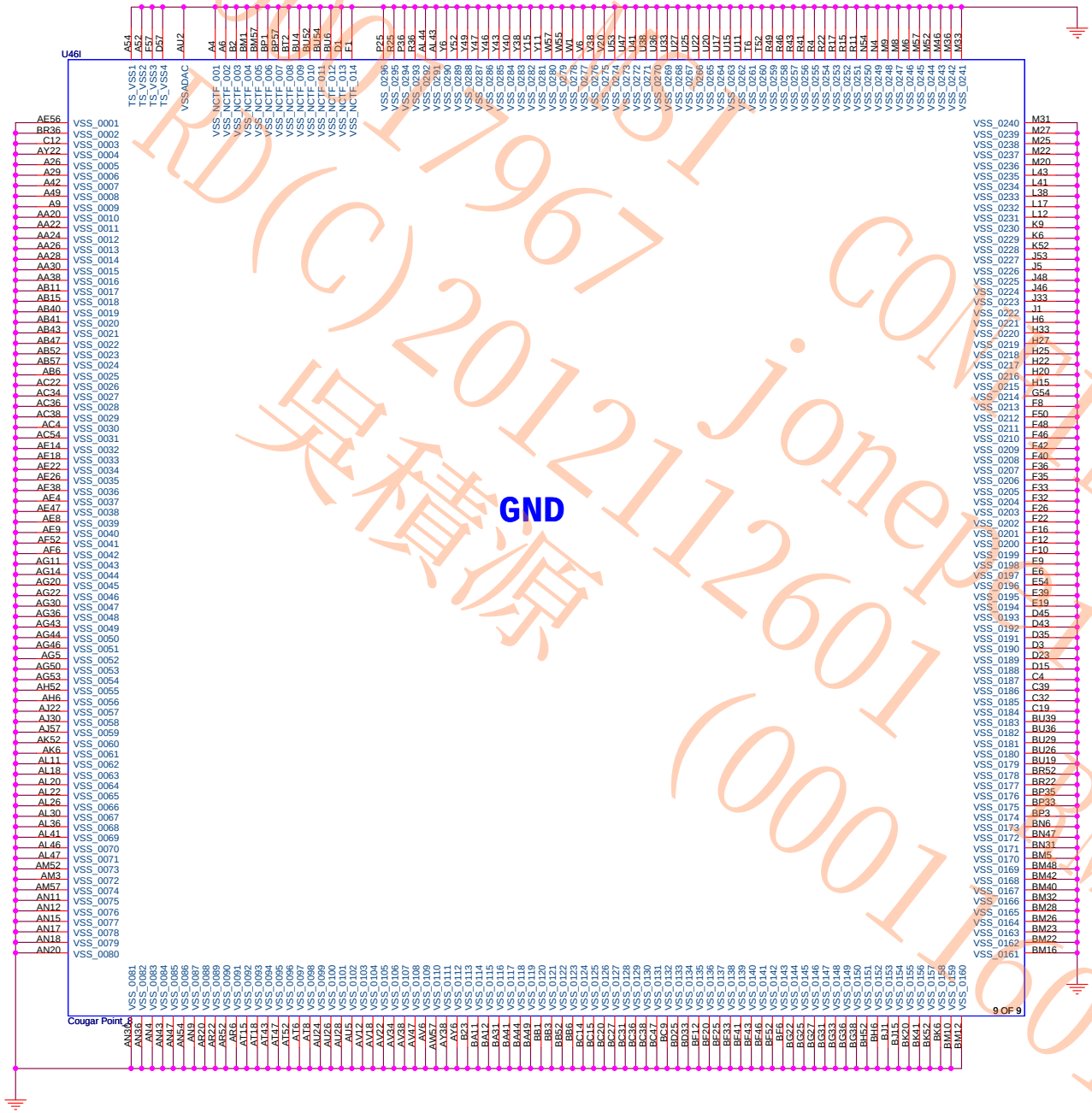

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RD(C)20121126 01 jonepi(裴亮樂)
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Size: Custom	Document Description: PPT-GND/NVRAM/USB30	Rev: 0A
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PCH Straps

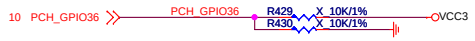
SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:

Internal pull-up

Do not pull low.

HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

Internal weak pull down. Do not pull up.



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by softstrap through ME.

Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

Internal weak pull up. Do not pull low.
On die PLL voltage regulator

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MS-7808

Size	Document Description	Rev
Custom	PPT Strap	0A

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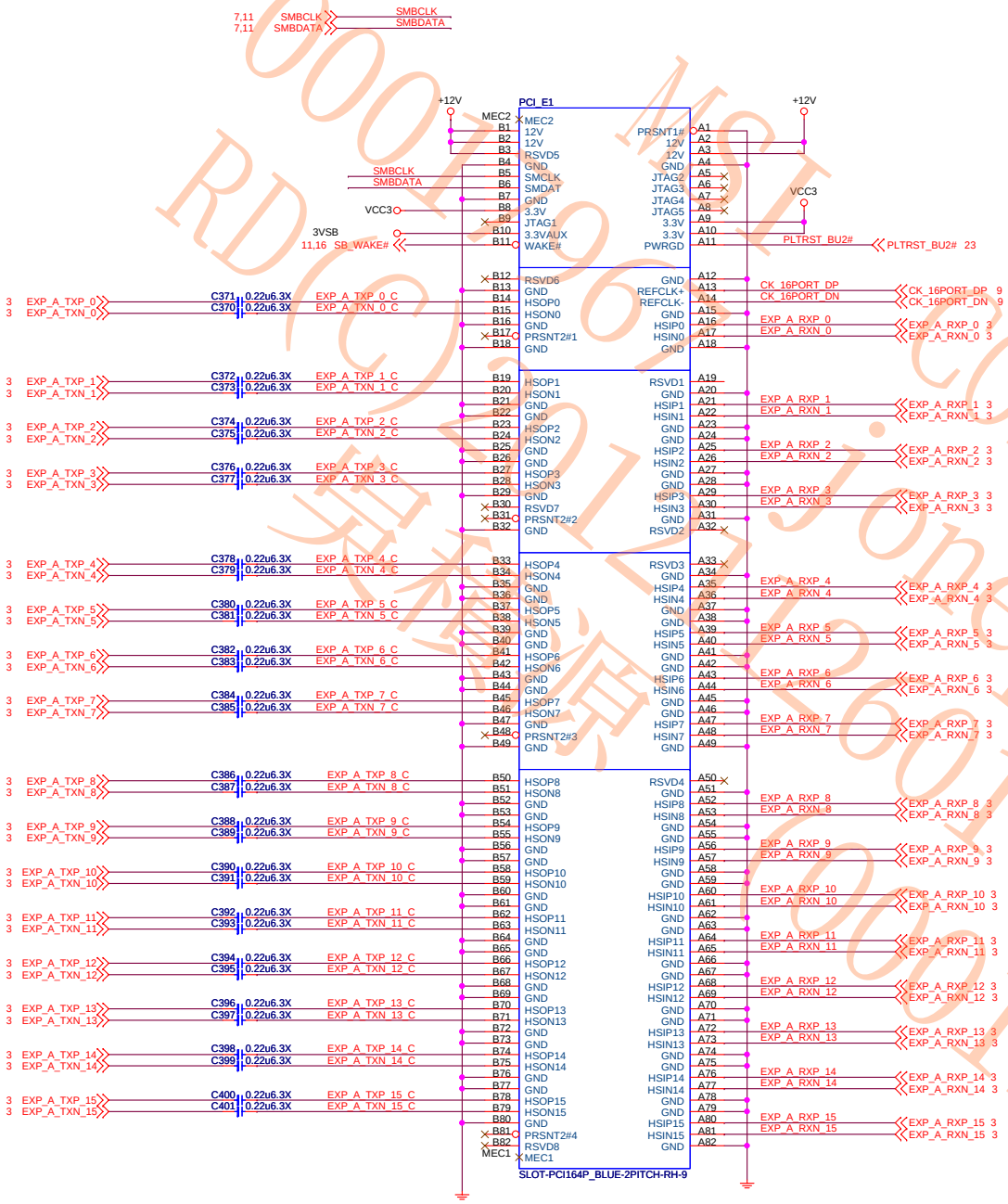
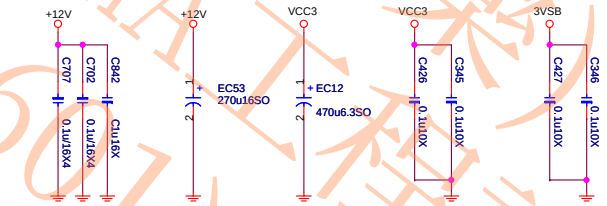


12V: 5.5A
VCC3: 3A
3VSB_WAKE: 0.375A



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RMA工程部(0001160)
MSI 微星科技股份有限公司

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Size: Custom	Document Description: PCIE1(X16) Slots
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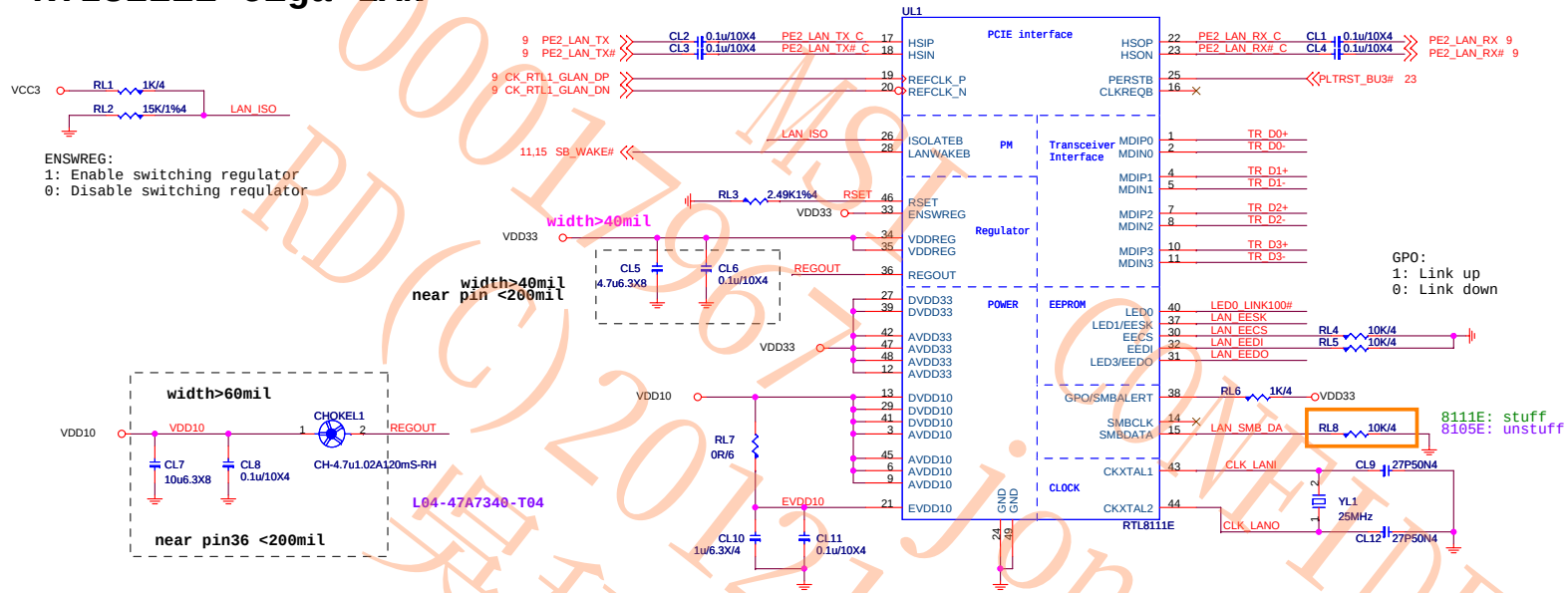
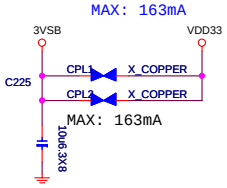
RTL8111E Giga LAN



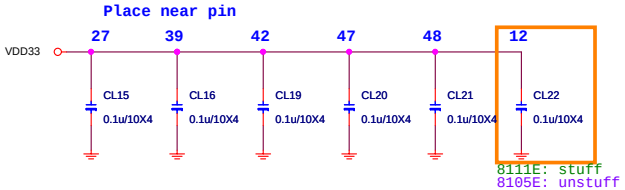
Pin49: 9 via from top layer to GND layer
and make the via at the center of IC.

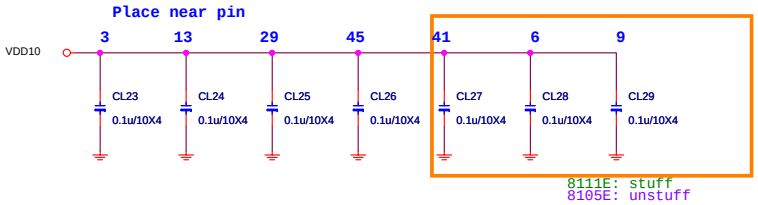


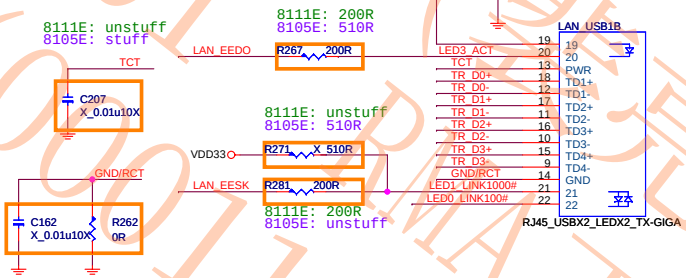
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

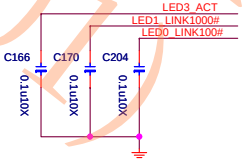
3.3v Power on rise time : 1~100ms.



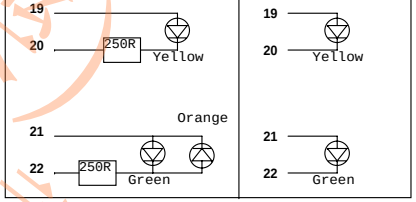




only support LED0+LED1/LED1+LED3 dual color LED
combinations when using EEPROM



Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None



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MS-7733	
Size: Custom	Document Description: LAN-RTL8111E/8105E
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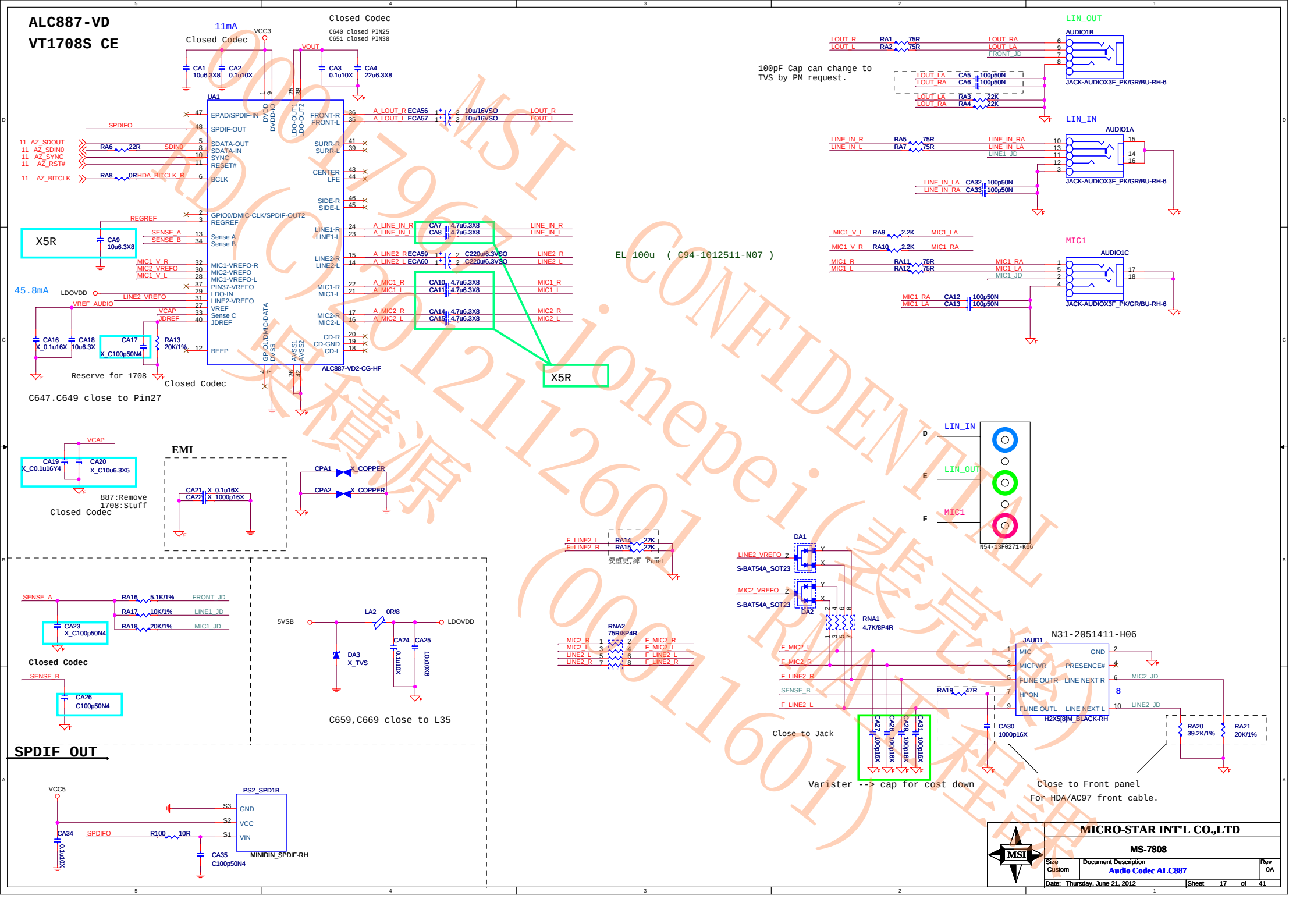
ALC887-VD
VT1708S CE
11mA
Closed Codec
Closed Codec
C640 closed PIN25
C651 closed PIN38
VCC3
VOUT
CA1 10u6.3X8
CA2 0.1u10X
CA3 0.1u10X
CA4 22u6.3X8
UA1
EPAD/SPDIF-IN
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
Sense A
Sense B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
BEEP
GPIO1/DMIC-DATA
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
DVSS
AVSS1
AVSS2
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
ALC887-VD2-CG-HF
SPDIFO
11 AZ_SDOUT
11 AZ_SDIN0
11 AZ_SYNC
11 AZ_RST#
11 AZ_BITCLK
RA6 22R SDIN0
RA8 0R HDA_BITCLK_R
REGREF
SENSE_A
SENSE_B
X5R
CA9 10u6.3X8
MIC1_V_R
MIC2_VREFO
MIC1_V_L
45.8mA
LDOVDD
LINE2_VREFO
VREF_AUDIO
VCAP
JDREF
CA16 X_0.1u16X
CA18 10u6.3X
CA17 X_C100p50N4
RA13 20K/1%
Reserve for 1708
Closed Codec
C647.C649 close to Pin27
A_LOUT_R ECA56 10u/16VSO LOUT_R
A_LOUT_L ECA57 10u/16VSO LOUT_L
A_LINE_IN_R CA7 4.7u6.3X8 LINE_IN_R
A_LINE_IN_L CA8 4.7u6.3X8 LINE_IN_L
A_LINE2_R ECA59 C220u/6.3VSO LINE2_R
A_LINE2_L ECA60 C220u/6.3VSO LINE2_L
A_MIC1_R CA10 4.7u6.3X8 MIC1_R
A_MIC1_L CA11 4.7u6.3X8 MIC1_L
A_MIC2_R CA14 4.7u6.3X8 MIC2_R
A_MIC2_L CA15 4.7u6.3X8 MIC2_L
X5R
EL 100u (C94-1012511-N07)
LIN_OUT
AUDIO1B
LOUT_R RA1 75R LOUT_RA
LOUT_L RA2 75R LOUT_LA
FRONT_JD
100pF Cap can change to
TVS by PM request.
LOUT_LA CA5 100p50N
LOUT_RA CA6 100p50N
LOUT_LA RA3 22K
LOUT_RA RA4 22K
JACK-AUDIOX3F_PK/GR/BU-RH-6
LIN_IN
AUDIO1A
LINE_IN_R RA5 75R LINE_IN_RA
LINE_IN_L RA7 75R LINE_IN_LA
LINE1_JD
LINE_IN_LA CA32 100p50N
LINE_IN_RA CA33 100p50N
JACK-AUDIOX3F_PK/GR/BU-RH-6
MIC1_V_L RA9 2.2K MIC1_LA
MIC1_V_R RA10 2.2K MIC1_RA
MIC1_R RA11 75R MIC1_RA
MIC1_L RA12 75R MIC1_LA
MIC1_JD
MIC1
AUDIO1C
MIC1_RA CA12 100p50N
MIC1_LA CA13 100p50N
JACK-AUDIOX3F_PK/GR/BU-RH-6
VCAP
CA19 X_C0.1u16Y4
CA20 X_C10u6.3X5
887:Remove
1708:Stuff
Closed Codec
EMI
CA21 X_0.1u16X
CA22 X_1000p16X
CPA1 X_COPPER
CPA2 X_COPPER
LIN_IN
LIN_OUT
MIC1
N54-13F0271-K06
F_LINE2_L RA14 22K
F_LINE2_R RA15 22K
安裝更,綁 Panel
DA1
LINE2_VREFO
S-BAT54A_SOT23
MIC2_VREFO
S-BAT54A_SOT23
DA2
RNA1 4.7K/8P4R
RNA2 75R/8P4R
MIC2_R F_MIC2_R
MIC2_L F_MIC2_L
LINE2_L F_LINE2_L
LINE2_R F_LINE2_R
N31-2051411-H06
JAUD1
MIC GND
MICPWR PRESENCE#
FLINE OUTR LINE NEXT R
HPON
FLINE OUTL LINE NEXT L
H2X5[8]M_BLACK-RH
F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
RA19 47R
CA30 1000p16X
CA27 100p16X
CA28 100p16X
CA29 100p16X
CA31 100p16X
Close to Jack
Varister --> cap for cost down
MIC2_JD
LINE2_JD
RA20 39.2K/1%
RA21 20K/1%
Close to Front panel
For HDA/AC97 front cable.
SENSE_A
RA16 5.1K/1% FRONT_JD
RA17 10K/1% LINE1_JD
RA18 20K/1% MIC1_JD
CA23 X_C100p50N4
Closed Codec
SENSE_B
CA26 C100p50N4
5VSB
LA2 0R/8
LDOVDD
DA3 X_TVS
CA24 0.1u10X
CA25 10u10X
C659,C669 close to L35
SPDIF OUT
VCC5
PS2_SPD1B
S3 GND
S2 VCC
S1 VIN
CA34 0.1u10X
SPDIFO
R100 10R
CA35 C100p50N4
MINIDIN_SPDIF-RH
MICRO-STAR INT'L CO.,LTD
MS-7808
Size Custom
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Rev 0A
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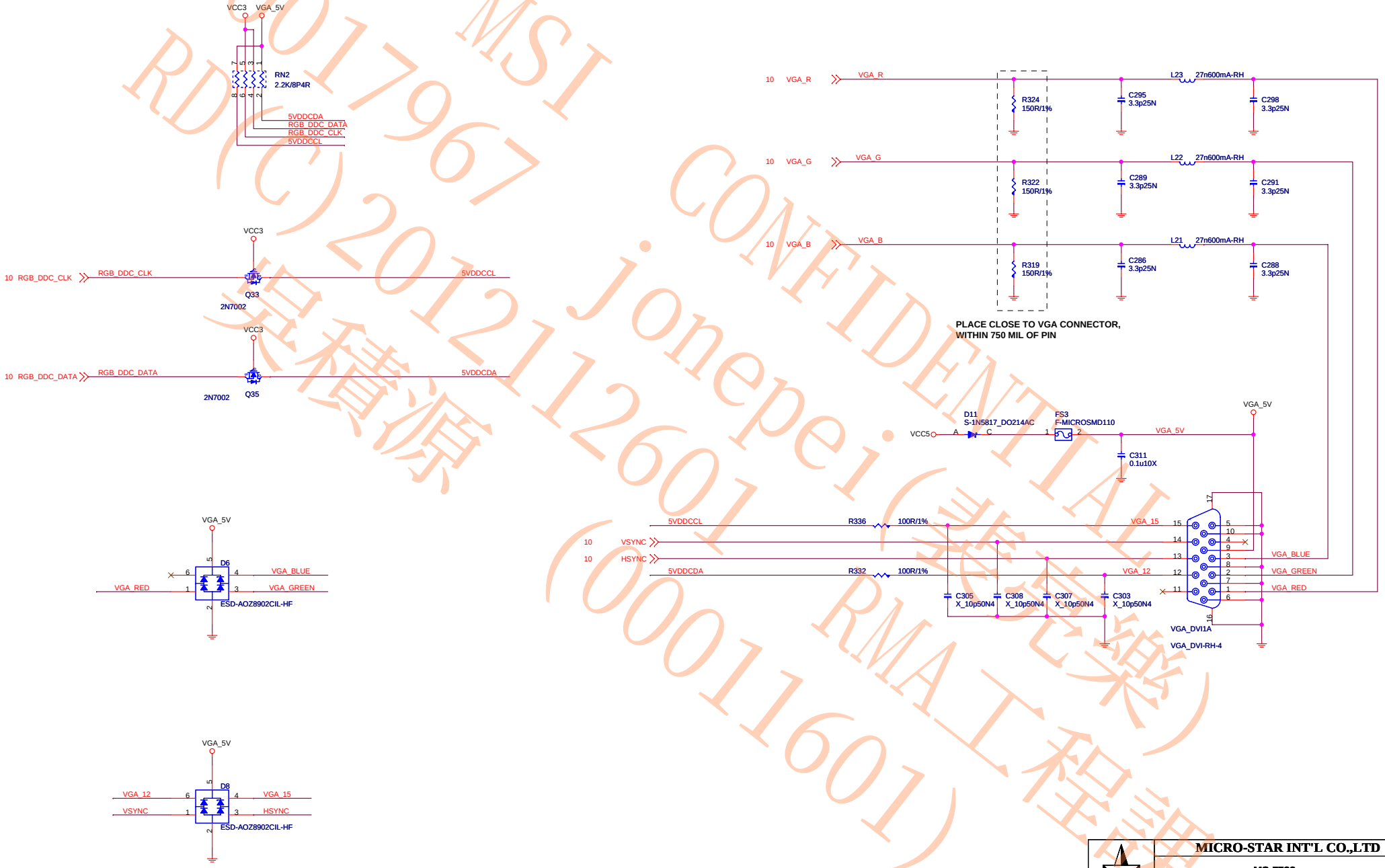
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



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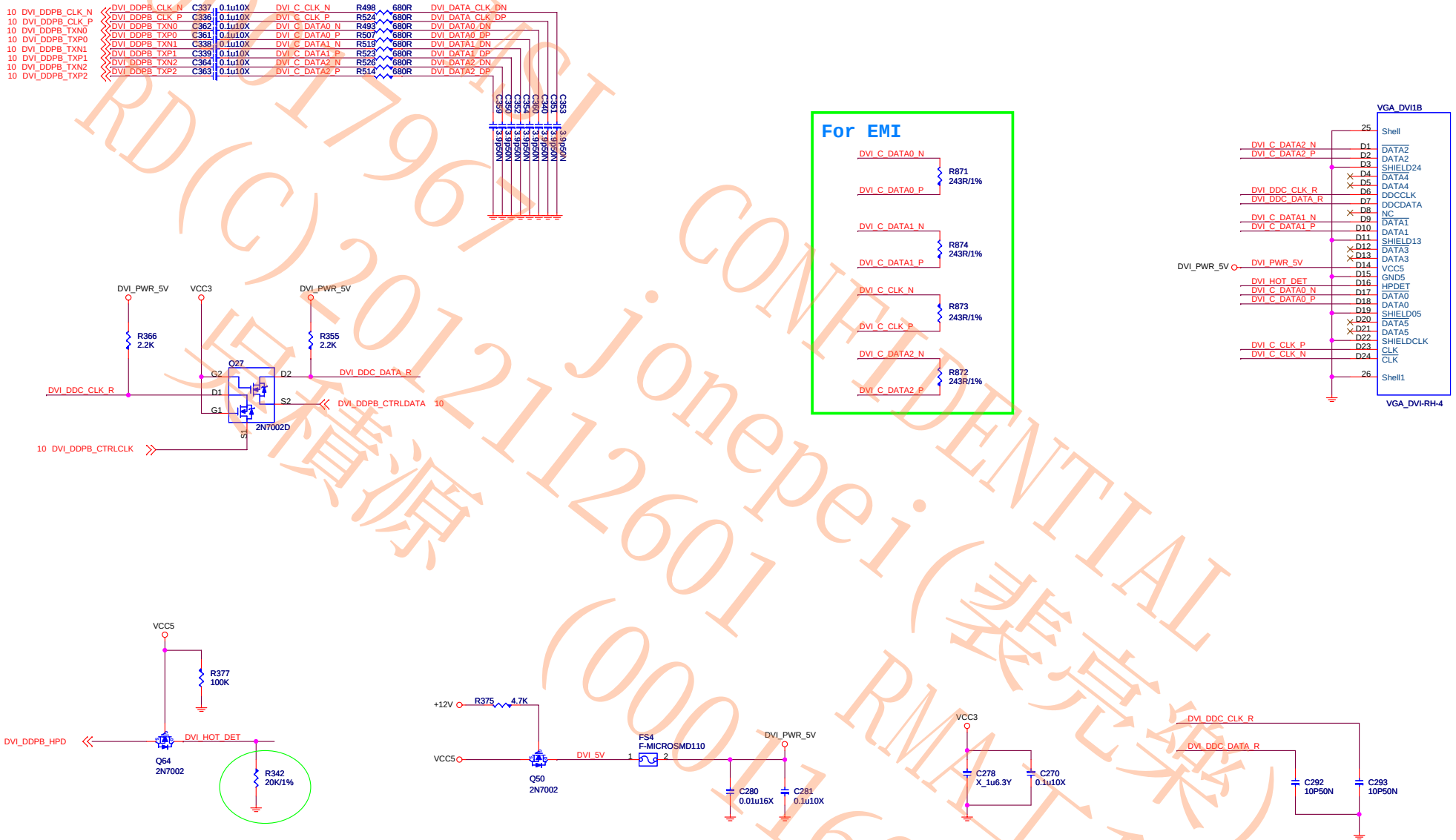
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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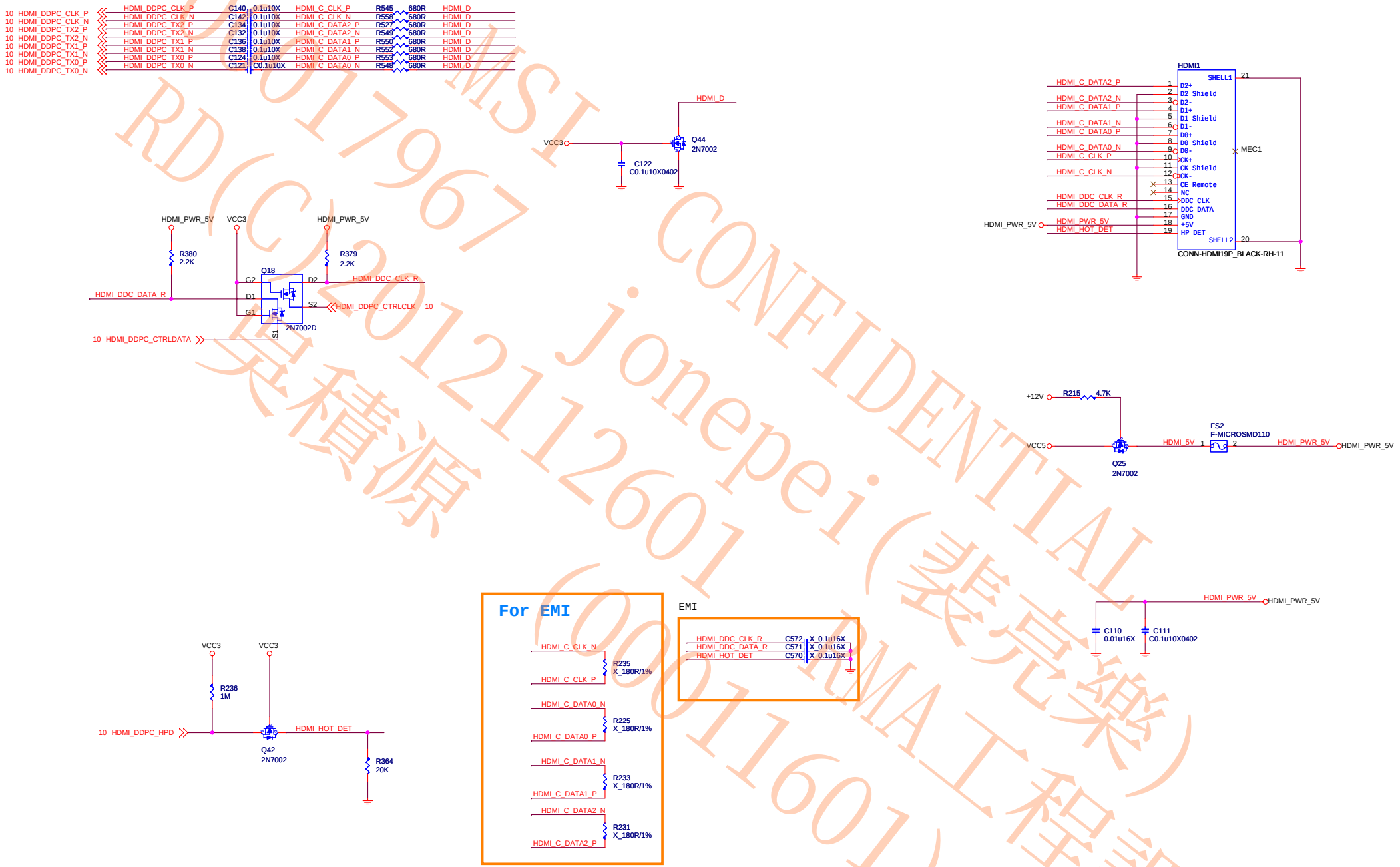
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



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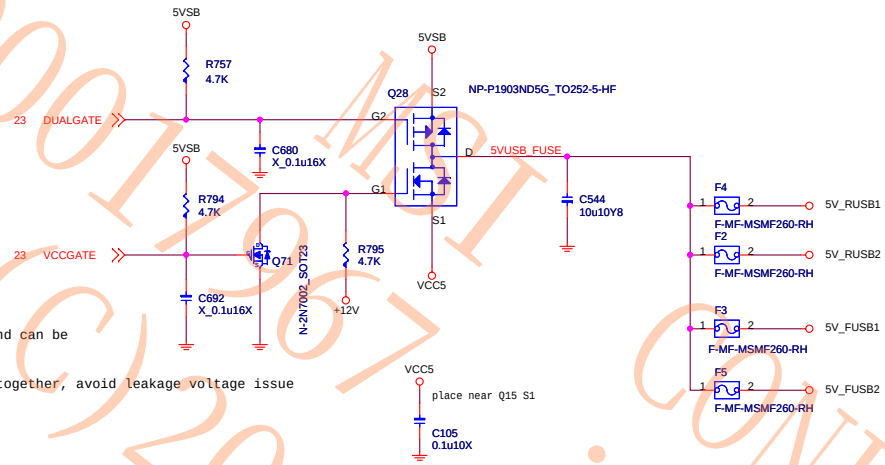
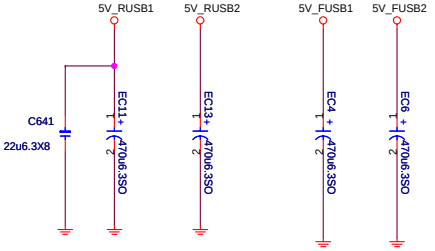
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

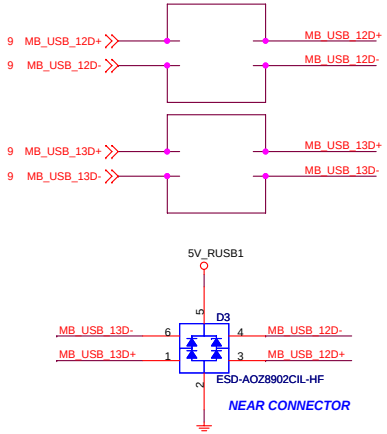
*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

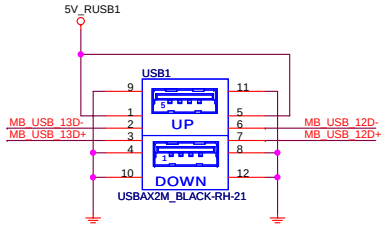
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



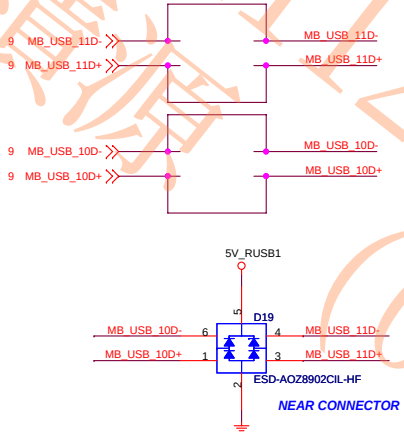


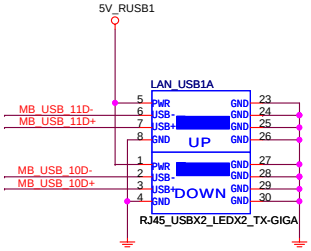
REAR USB PORT 12,13



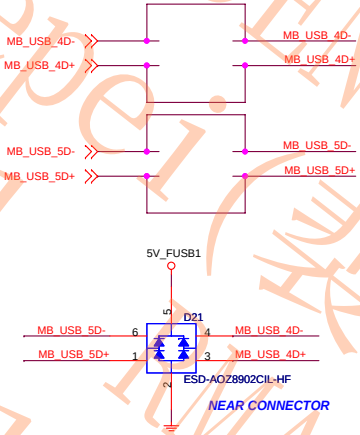


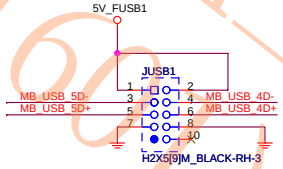
FRONT USB PORT 10,11(With LAN)



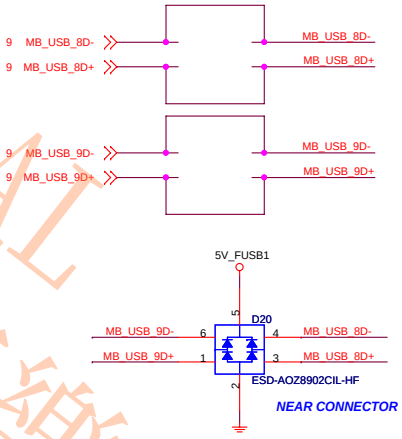


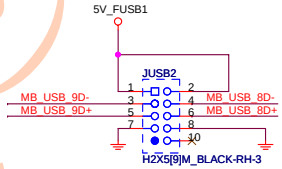
FRONT USB PORT 4.5





FRONT USB PORT 8.9





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吳德源 (MA工程師)

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Size: Custom	Document Description: Rear I/O & USB2.0 Connector	Rev: 30
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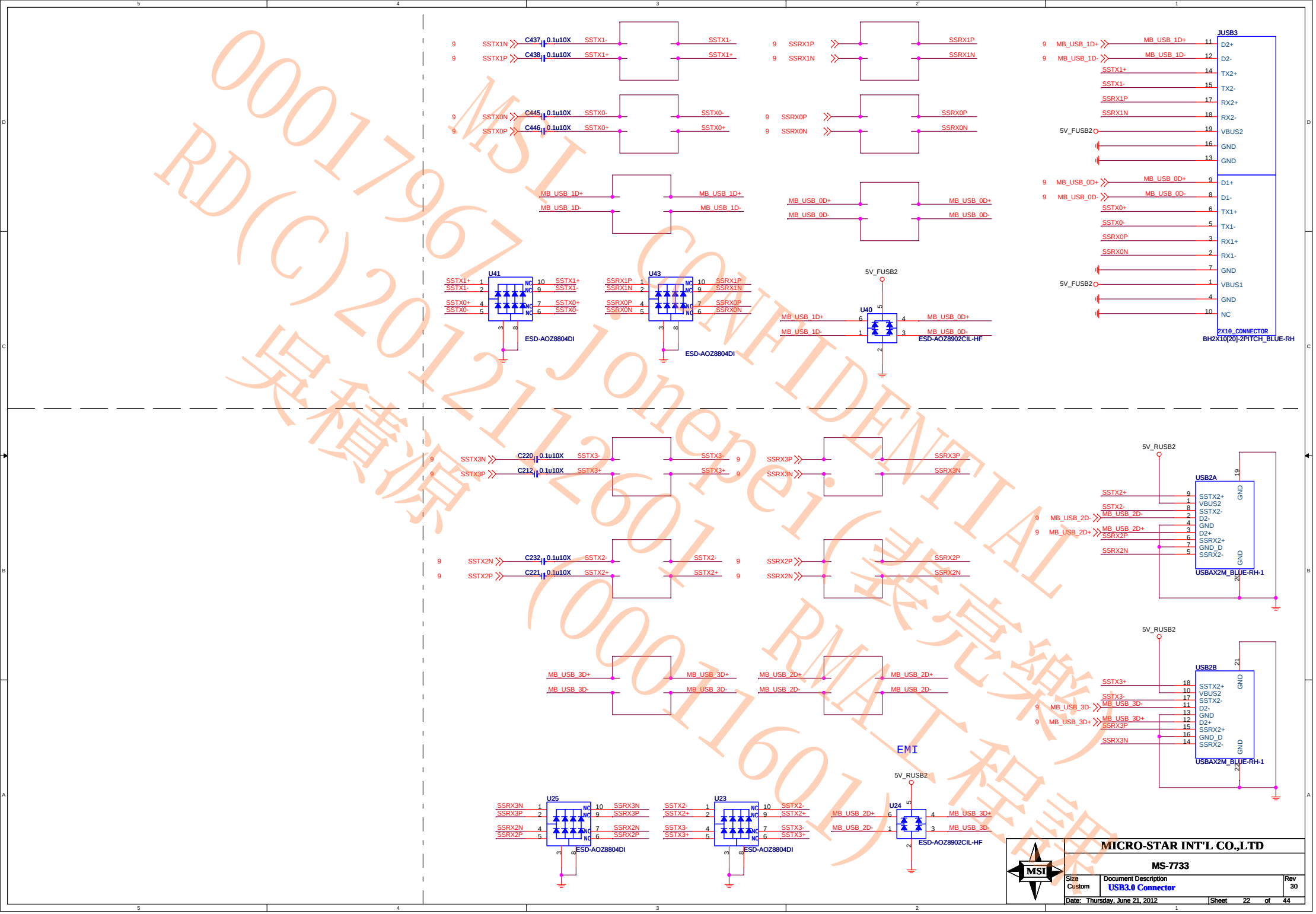

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Size	Document Description	Rev
Custom	USB3.0 Connector	30

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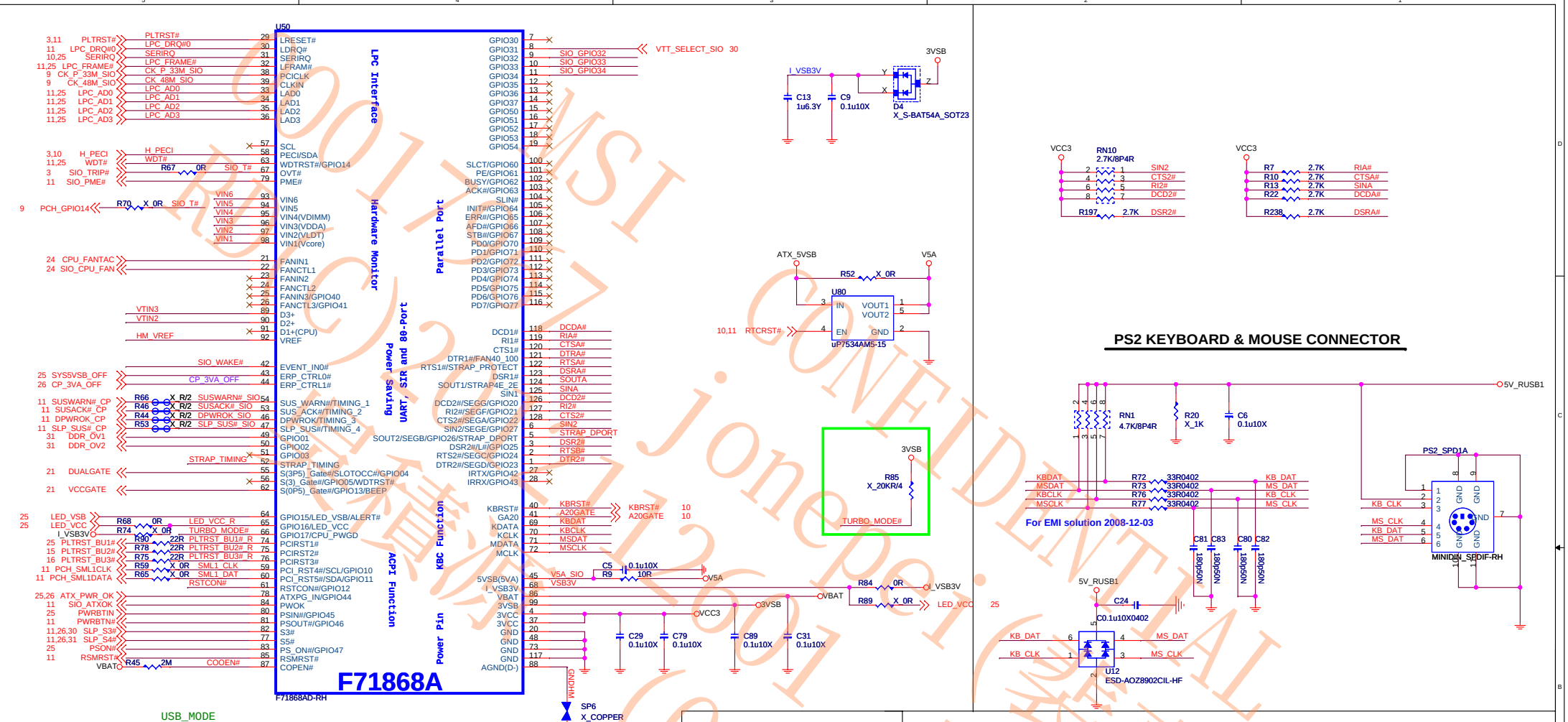
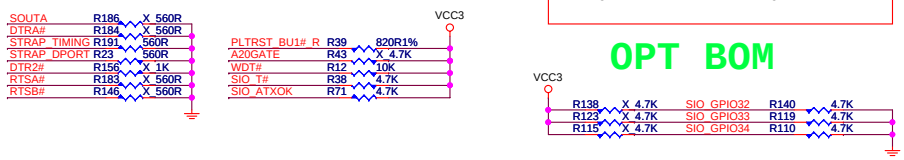
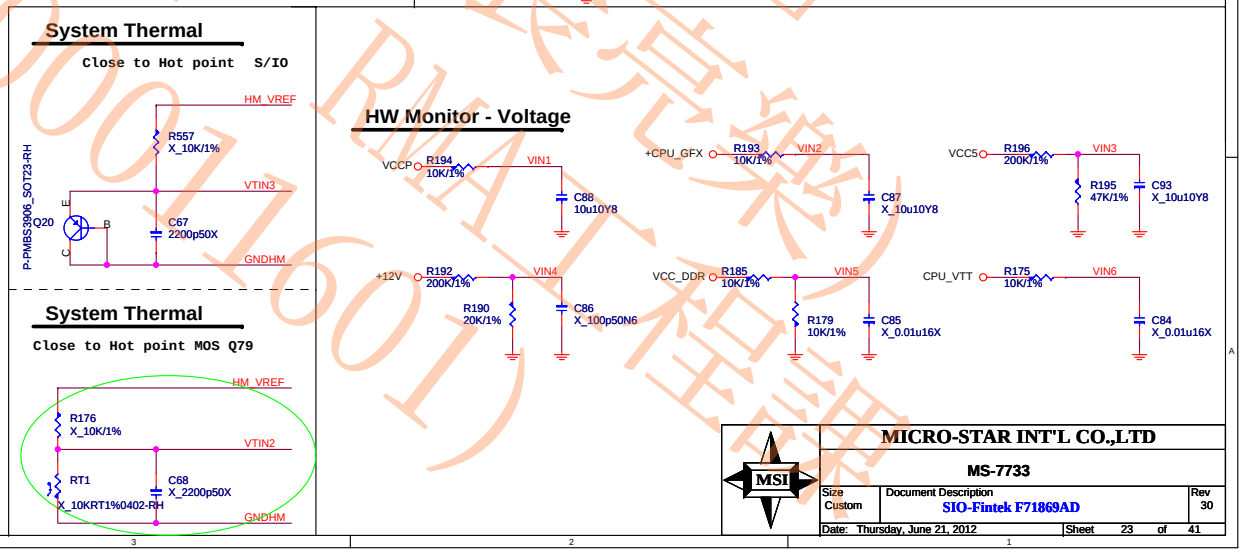
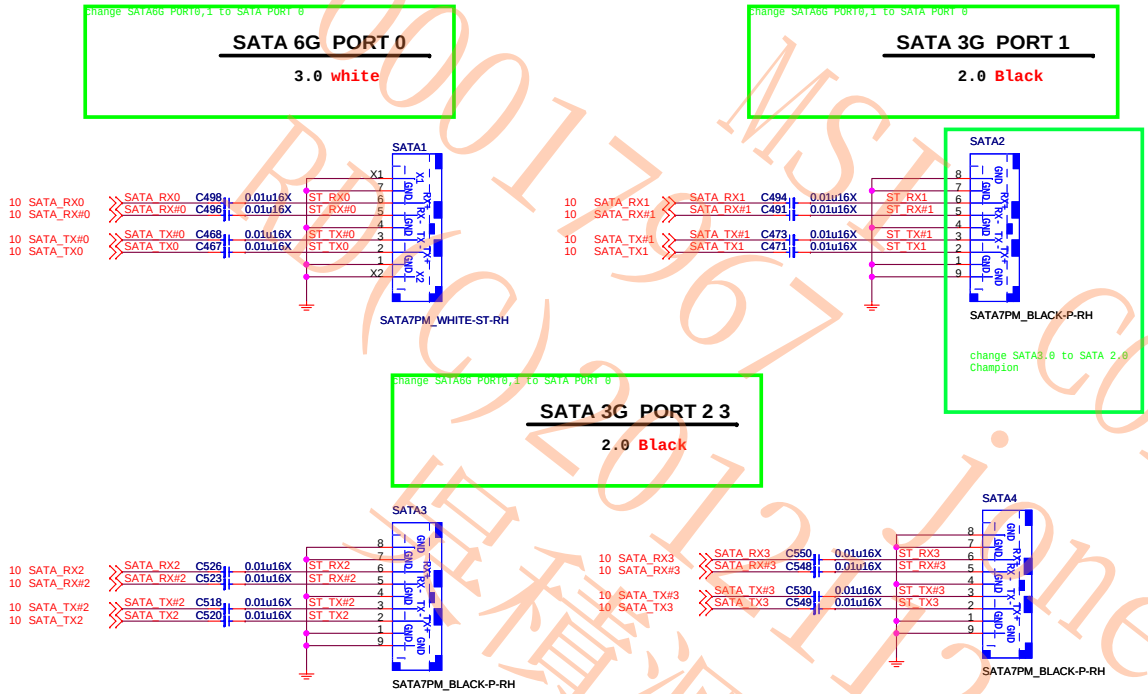


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

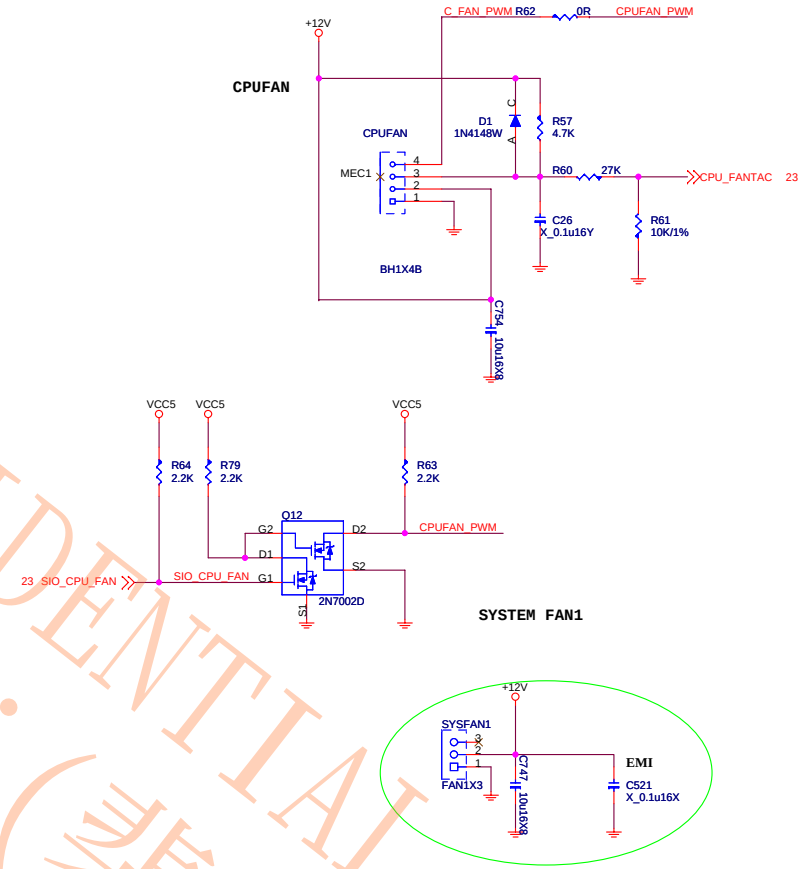
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		







FAN-COUNTROL CIRCUIT



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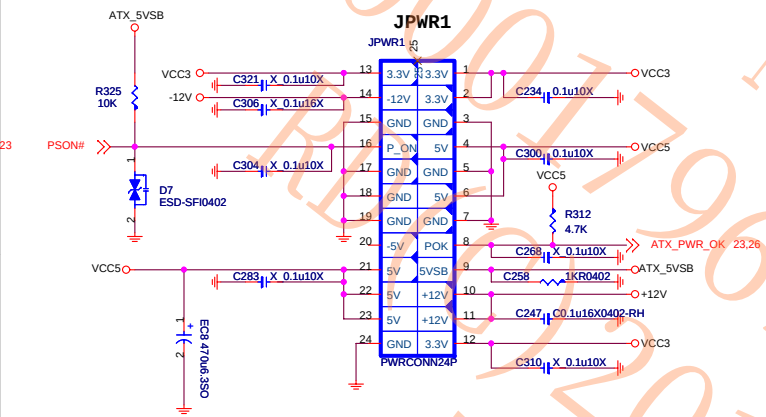
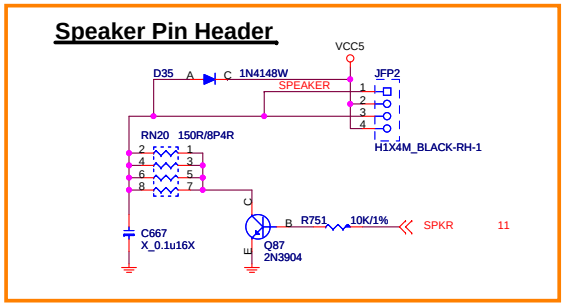
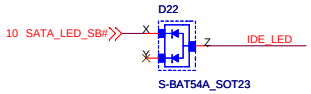
ATX POWER CONNECTOR

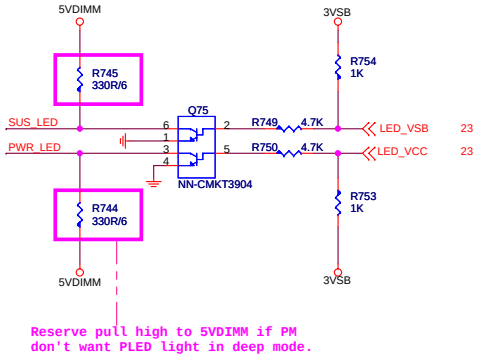


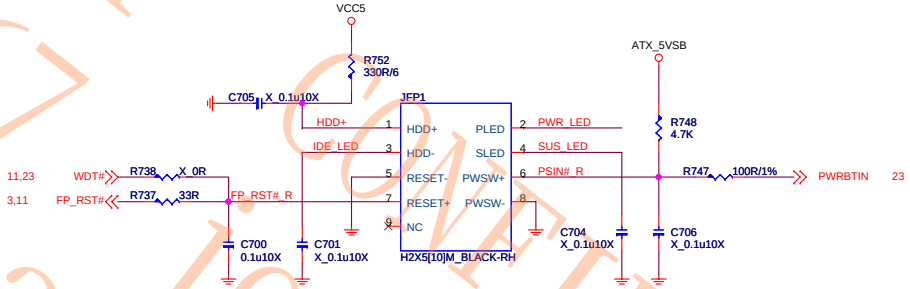
Speaker Pin Header





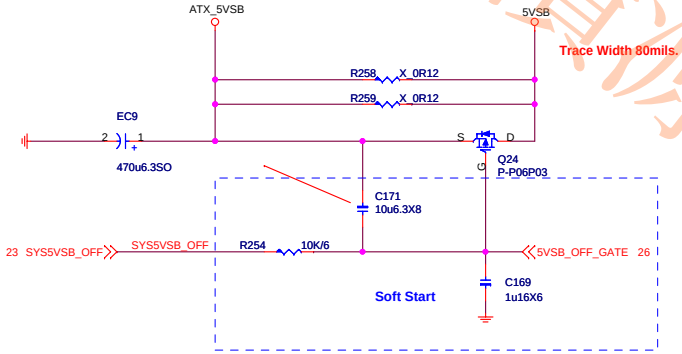
LED (for Fintek 71869)



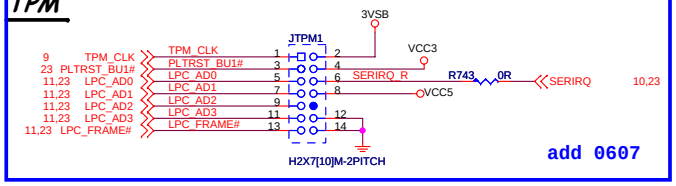


5VSB Power Switch

Tune 5VSB inrush current to 2A from 4A



TPM



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(00011601)
(00011967 是積源 RMA工程師)

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Size: Custom	Document Description: ATX F_Panel/EMI/TPM	Rev: 30
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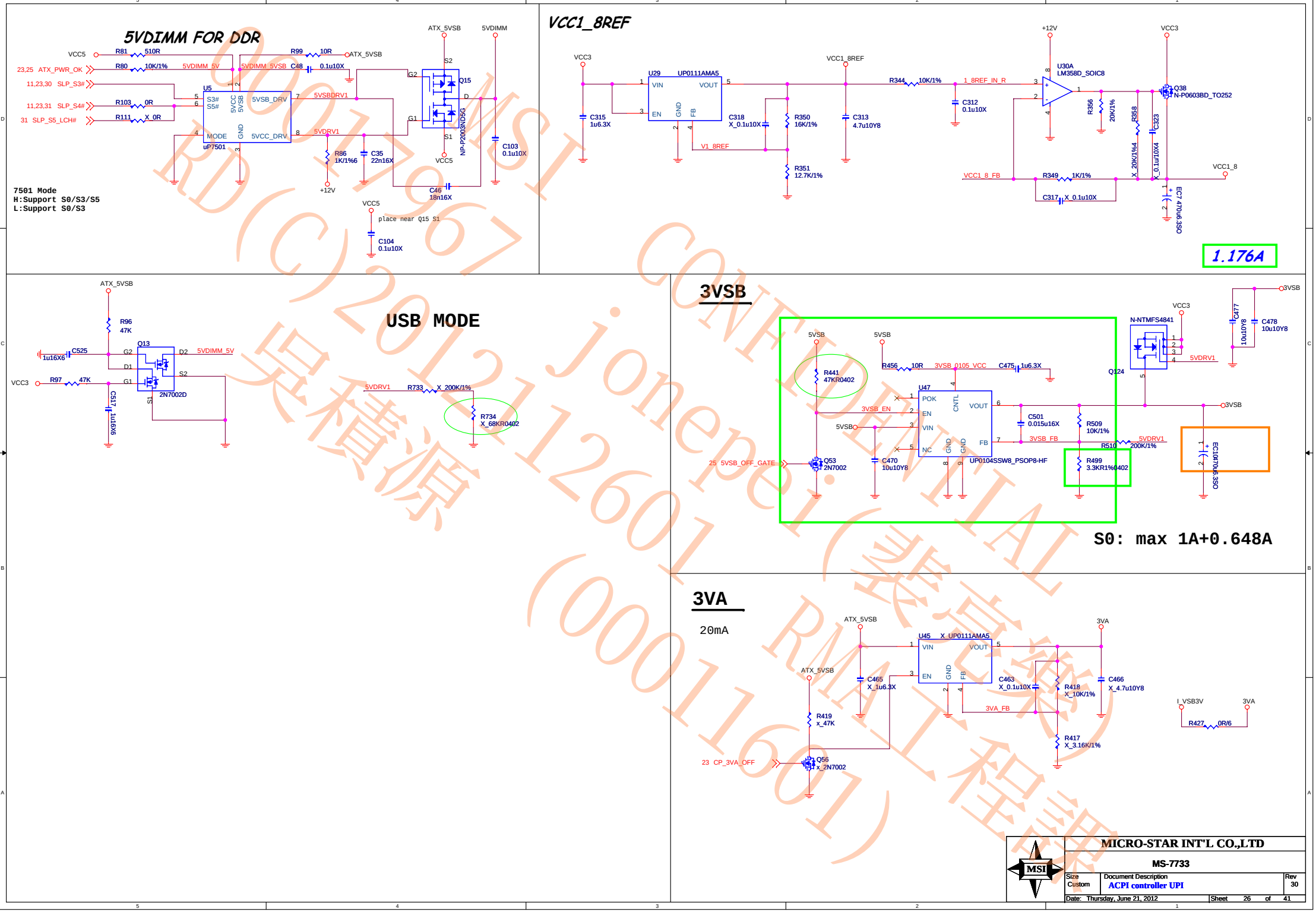

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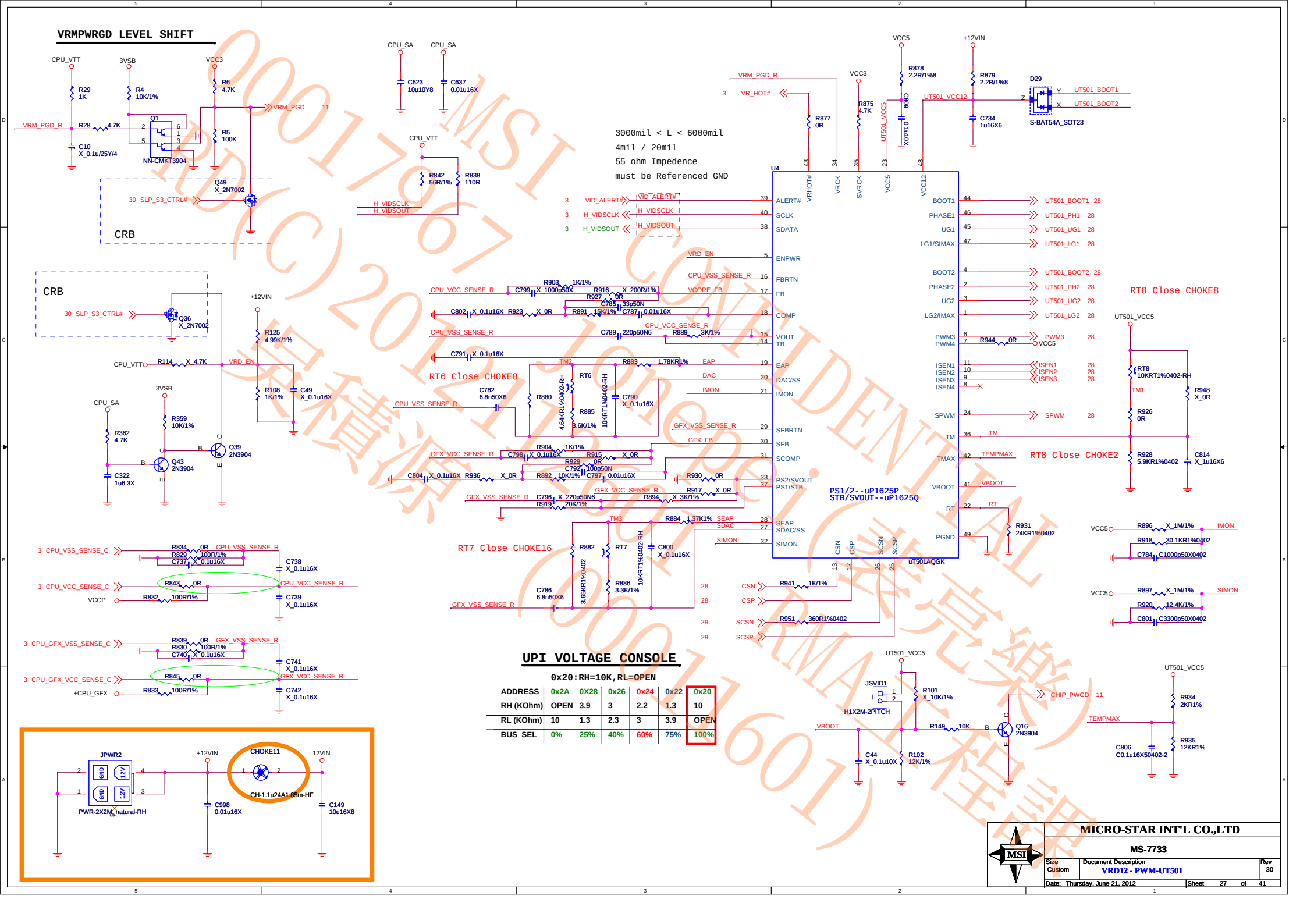
VRMPWRGD LEVEL SHIFT
CPU_VTT
3VSB
VCC3
R29 1K
R4 10K/1%
R6 4.7K
R5 100K
VRM_PGD_R
R28 4.7K
C10 X_0.1u/25Y/4
Q1
NN-CMKT3904
VRM_PGD
Q49 X_2N7002
30 SLP_S3_CTRL#
CRB
CPU_SA
C623 10u10Y8
C637 0.01u16X
R842 56R/1%
R838 110R
H_VIDSCLK
H_VIDSOUT
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND
VRM_PGD_R
VR_HOT#
R877 0R
R875 4.7K
R878 2.2R/1%8
R879 2.2R/1%8
C809 0.1u10X
UT501_VCC12
C734 1u16X6
D29
S-BAT54A_SOT23
UT501_BOOT1
UT501_BOOT2
U4
VID_ALERT#
H_VIDSCLK
H_VIDSOUT
VRD_EN
CPU_VSS_SENSE_R
VCORE_FB
CPU_VCC_SENSE_R
EAP
DAC
IMON
GFX_VSS_SENSE_R
GFX_FB
GFX_VCC_SENSE_R
SEAP
SDAC
SIMON
CSN
CSP
SCSN
SCSP
ALERT#
SCLK
SDATA
ENPWR
FBRTN
FB
COMP
VOUT
TB
EAP
DAC/SS
IMON
SFBRTN
SFB
SCOMP
PS2/SVOUT
PS1/STB
SEAP
SDAC/SS
SIMON
VRHOT#
VROK
SVROK
VCC5
VCC12
BOOT1
PHASE1
UG1
LG1/SIMAX
BOOT2
PHASE2
UG2
LG2/IMAX
PWM3
PWM4
ISEN1
ISEN2
ISEN3
ISEN4
SPWM
TM
TMAX
VBOOT
RT
PGND
UT501_BOOT1 28
UT501_PH1 28
UT501_UG1 28
UT501_LG1 28
UT501_BOOT2 28
UT501_PH2 28
UT501_UG2 28
UT501_LG2 28
PWM3 28
ISEN1 28
ISEN2 28
ISEN3 28
SPWM 28
TEMPMAX
VBOOT
RT
PS1/2--uP1625P
STB/SVOUT--uP1625Q
uT501AQGK
RT6 Close CHOKE8
RT7 Close CHOKE16
RT8 Close CHOKE8
RT8 Close CHOKE2
R931 24KR1%0402
R941 1K/1%
R951 360R1%0402
R896 X_1M/1%
R918 30.1KR1%0402
C784 C1000p50X0402
R897 X_1M/1%
R920 12.4K/1%
C801 C3300p50X0402
CHIP_PWGD 11
R934 2KR1%
R935 12KR1%
C806 C0.1u16X50402-2
JSVID1
H1X2M-2PITCH
R101 X_10K/1%
R149 10K
Q16 2N3904
C44 X_0.1u10X
R102 12K/1%
3 CPU_VSS_SENSE_C
3 CPU_VCC_SENSE_C
VCCP
3 CPU_GFX_VSS_SENSE_C
3 CPU_GFX_VCC_SENSE_C
+CPU_GFX
JPWR2
PWR-2X2M-Natural-RH
+12VIN
CHOKE11
CH-1.1u24A1.85m-HF
12VIN
C998 0.01u16X
C149 10u16X8
UPI VOLTAGE CONSOLE
0x20:RH=10K,RL=OPEN
ADDRESS 0x2A 0x28 0x26 0x24 0x22 0x20
RH (KOhm) OPEN 3.9 3 2.2 1.3 10
RL (KOhm) 10 1.3 2.3 3 3.9 OPEN
BUS_SEL 0% 25% 40% 60% 75% 100%
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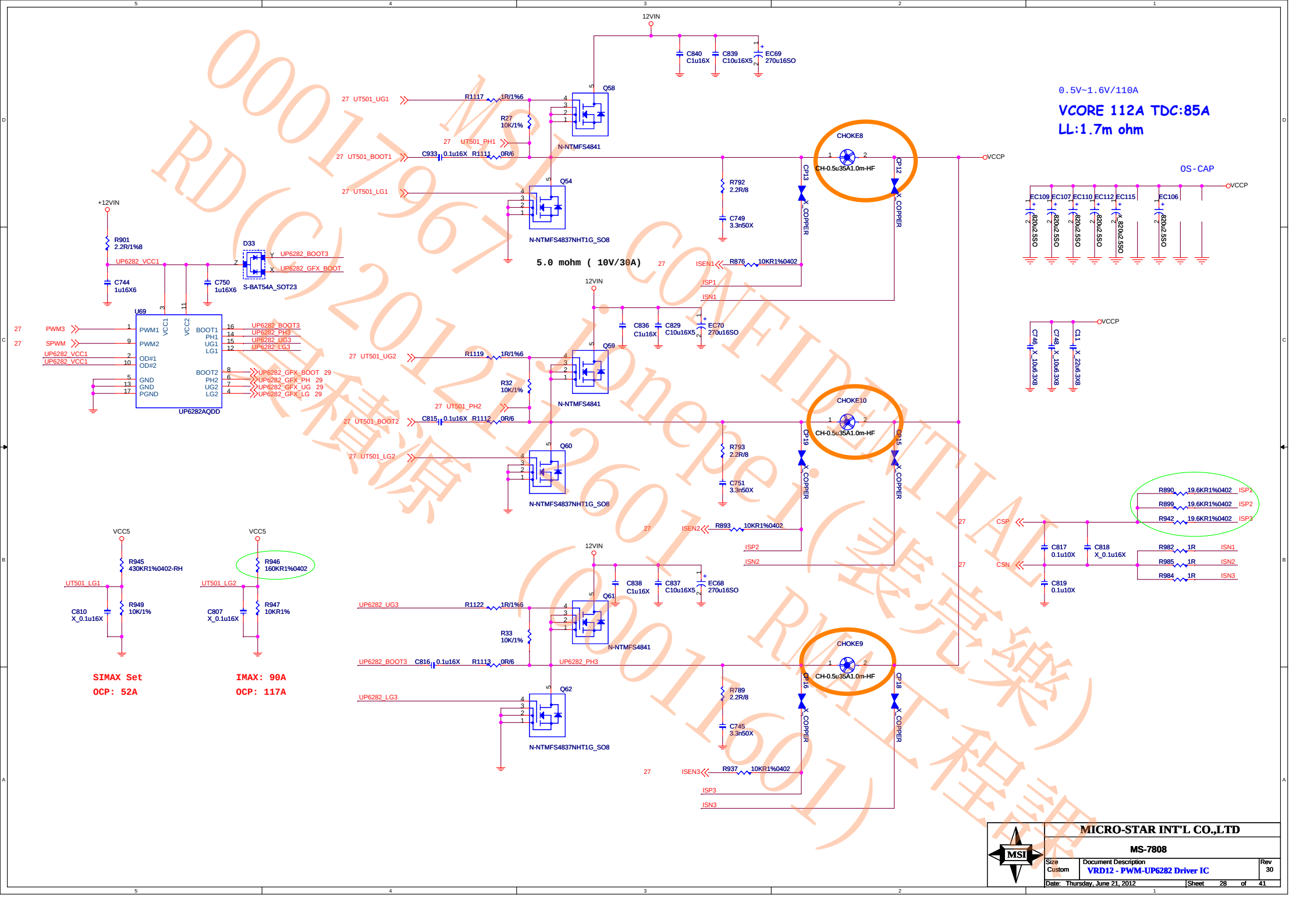
12VIN
C840 C1u16X
C839 C10u16X5
EC69 270u16SO
0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm
27 UT501_UG1
R1117 1R/1%6
R27 10K/1%
Q58
N-NTMFS4841
27 UT501_PH1
27 UT501_BOOT1
C933 0.1u16X
R1111 0R/6
27 UT501_LG1
Q54
N-NTMFS4837NHT1G_SO8
5.0 mohm (10V/30A)
CHOKE8
CH-0.5u35A1.0m-HF
CP13 X_COPPER
CP12 X_COPPER
VCCP
R792 2.2R/8
C749 3.3n50X
27 ISEN1
R876 10KR1%0402
ISP1
ISN1
OS-CAP
EC109 EC107 EC110 EC112 EC115 EC106
820u2.5SO
X_820u2.5SO
+12VIN
R901 2.2R/1%8
UP6282_VCC1
C744 1u16X6
C750 1u16X6
D33
S-BAT54A_SOT23
UP6282_BOOT3
UP6282_GFX_BOOT
U69
27 PWM3
27 SPWM
UP6282_VCC1
UP6282_VCC1
PWM1
PWM2
OD#1
OD#2
GND
GND
PGND
VCC1
VCC2
BOOT1
PH1
UG1
LG1
BOOT2
PH2
UG2
LG2
UP6282_BOOT3
UP6282_PH3
UP6282_UG3
UP6282_LG3
UP6282_GFX_BOOT 29
UP6282_GFX_PH 29
UP6282_GFX_UG 29
UP6282_GFX_LG 29
UP6282AQDD
12VIN
C836 C1u16X
C829 C10u16X5
EC70 270u16SO
27 UT501_UG2
R1119 1R/1%6
R32 10K/1%
Q59
N-NTMFS4841
27 UT501_PH2
27 UT501_BOOT2
C815 0.1u16X
R1112 0R/6
27 UT501_LG2
Q60
N-NTMFS4837NHT1G_SO8
CHOKE10
CH-0.5u35A1.0m-HF
CP19 X_COPPER
CP15 X_COPPER
R793 2.2R/8
C751 3.3n50X
27 ISEN2
R893 10KR1%0402
ISP2
ISN2
VCCP
C746 X_10u6.3X8
C748 X_10u6.3X8
C11 X_22u6.3X8
R890 19.6KR1%0402 ISP1
R899 19.6KR1%0402 ISP2
R942 19.6KR1%0402 ISP3
27 CSP
27 CSN
C817 0.1u10X
C818 X_0.1u16X
C819 0.1u10X
R982 1R ISN1
R985 1R ISN2
R984 1R ISN3
VCC5
R945 430KR1%0402-RH
UT501_LG1
R949 10K/1%
C810 X_0.1u16X
VCC5
R946 160KR1%0402
UT501_LG2
R947 10KR1%
C807 X_0.1u16X
SIMAX Set
OCP: 52A
IMAX: 90A
OCP: 117A
12VIN
C838 C1u16X
C837 C10u16X5
EC68 270u16SO
UP6282_UG3
R1122 1R/1%6
R33 10K/1%
Q61
N-NTMFS4841
UP6282_BOOT3
C816 0.1u16X
R1113 0R/6
UP6282_PH3
UP6282_LG3
Q62
N-NTMFS4837NHT1G_SO8
CHOKE9
CH-0.5u35A1.0m-HF
CP16 X_COPPER
CP18 X_COPPER
R789 2.2R/8
C745 3.3n50X
27 ISEN3
R937 10KR1%0402
ISP3
ISN3
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MS-7808
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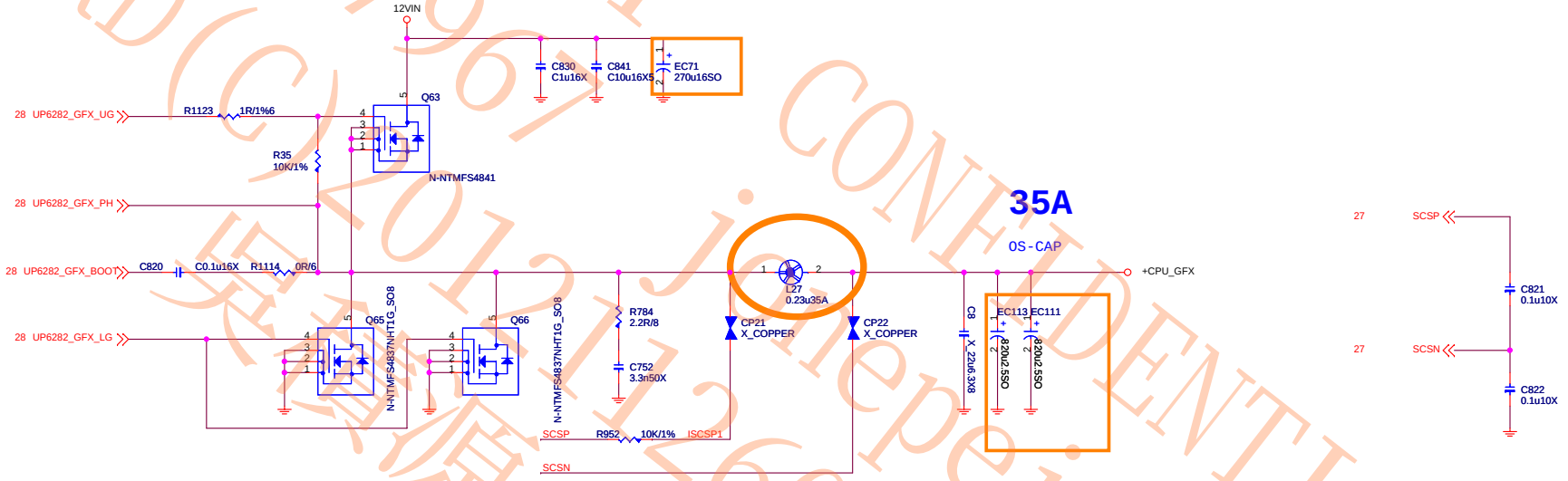
CPU_GFX:0.25-1.52

35A FOR CPU



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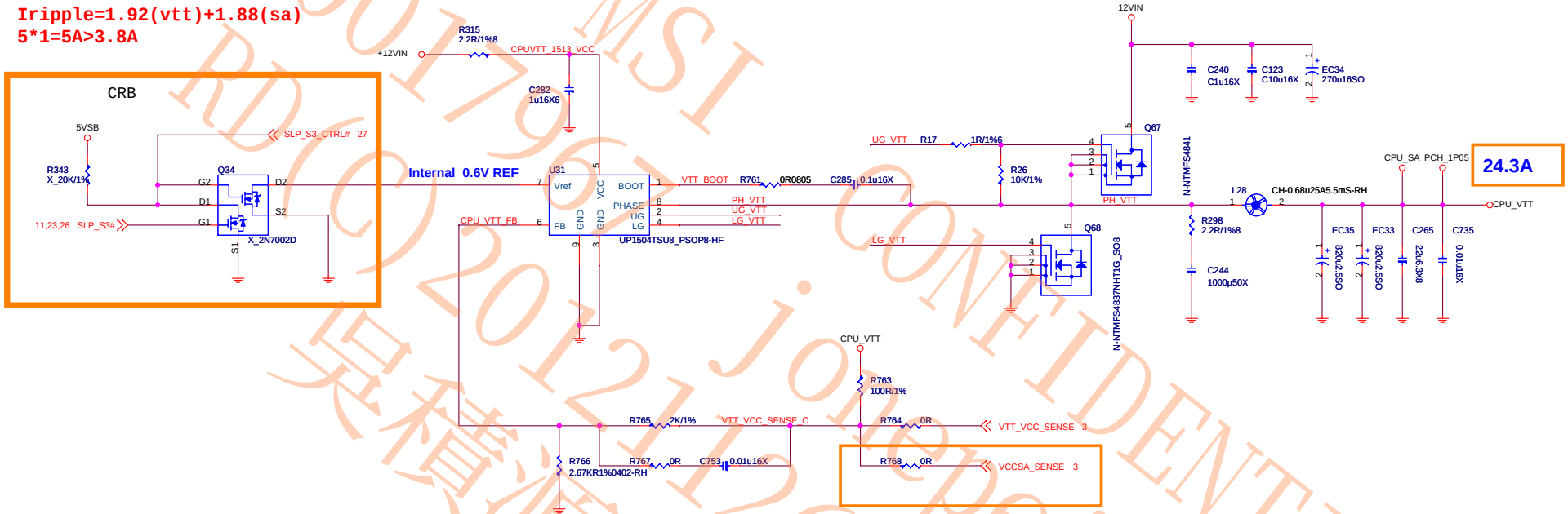
CPU_VTT:1.05/1.00 MAX 24.3A

CPU VTT 8.5A SA Core =8.8A PCH Core =7A

8.5A FOR CPU
Iripple=1.92(vtt)+1.88(sa)
5*1=5A>3.8A

Iripple=6.2
4.7*1A<6.2A share with VCCP

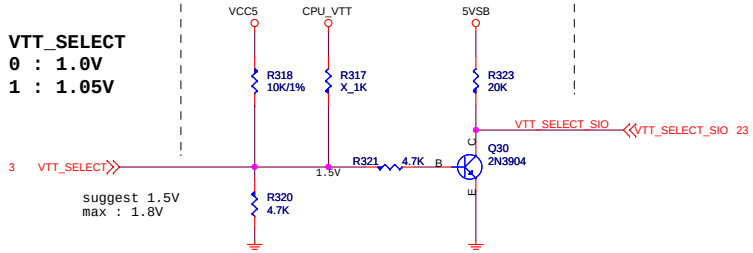
Acture measure cpu_vtt max 10A
Iripple=2.55A

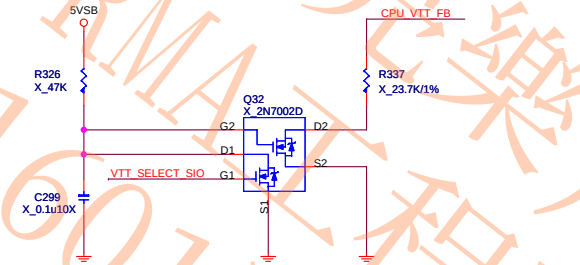


VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

VTT_SELECT
0 : 1.0V
1 : 1.05V





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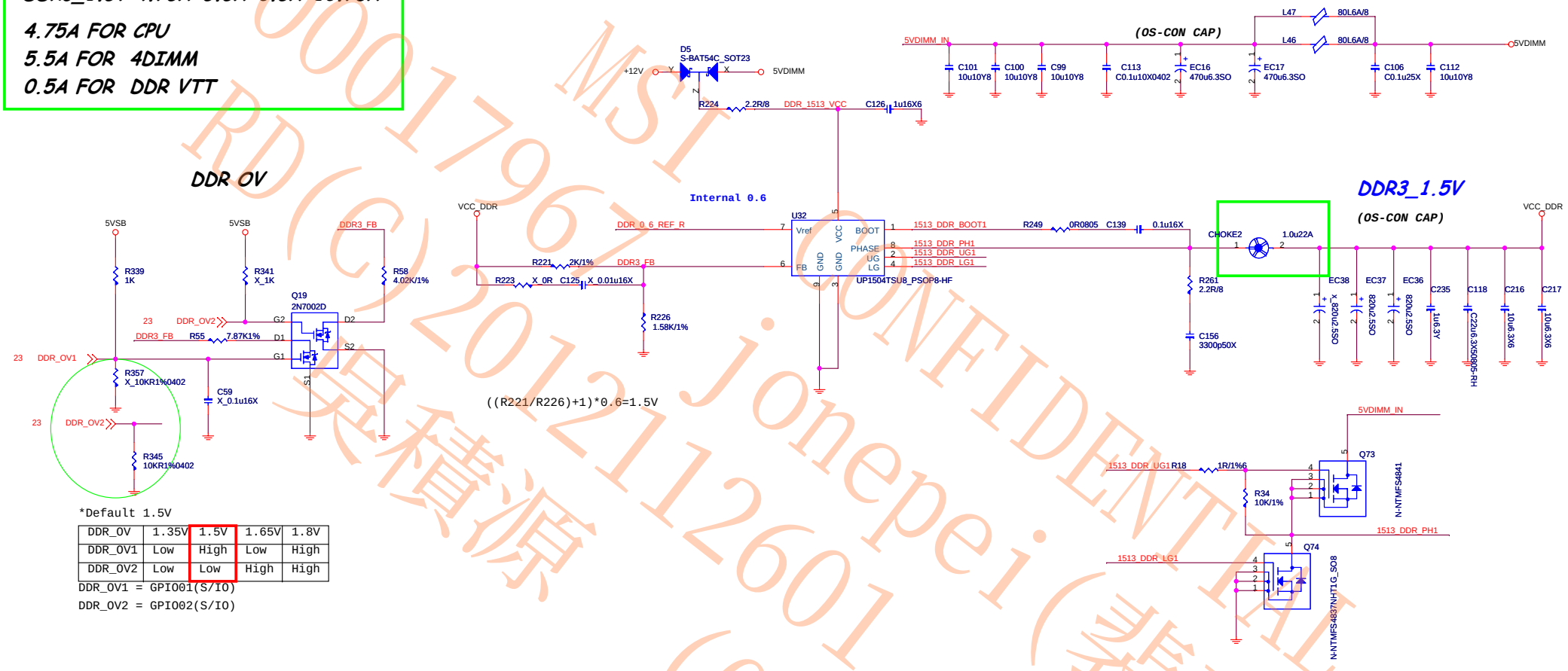
DDR Power:1.5V

DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU
5.5A FOR 4DIMM
0.5A FOR DDR VTT

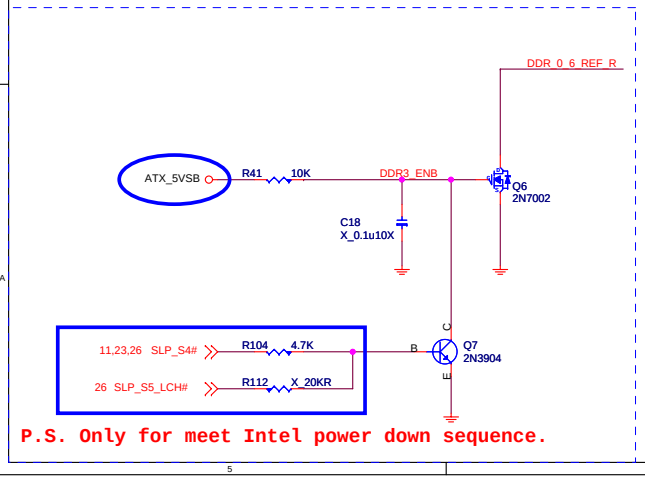
Iripple=4.868
4.7*2*1=9.4A>4.868A



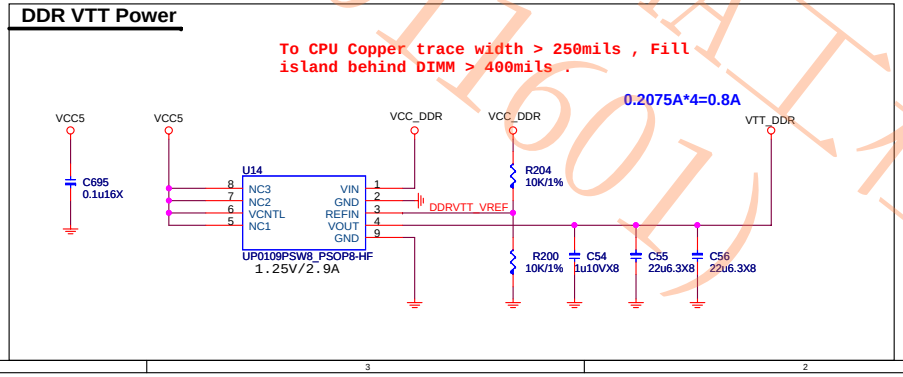
*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)



P.S. Only for meet Intel power down sequence.



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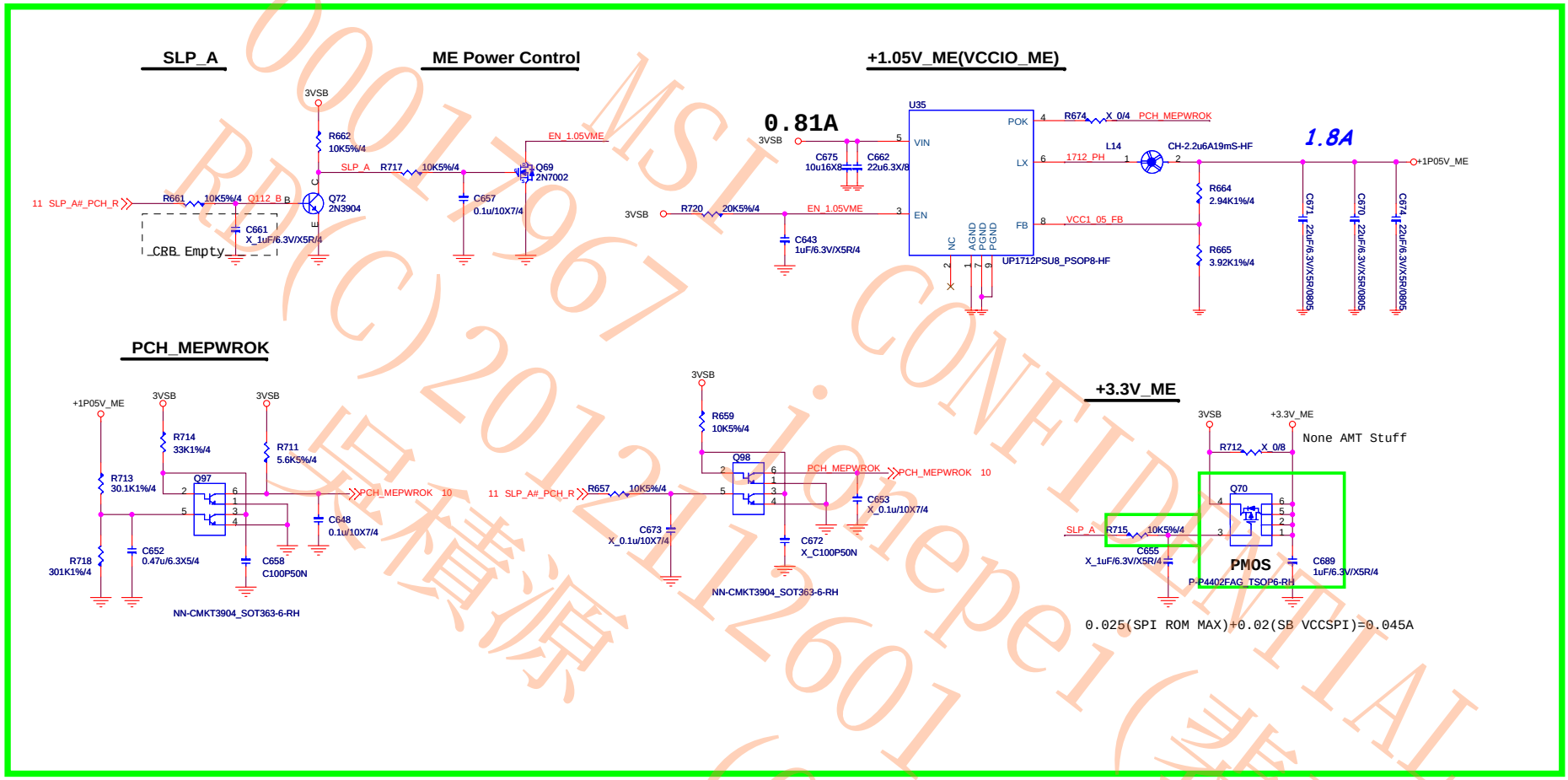

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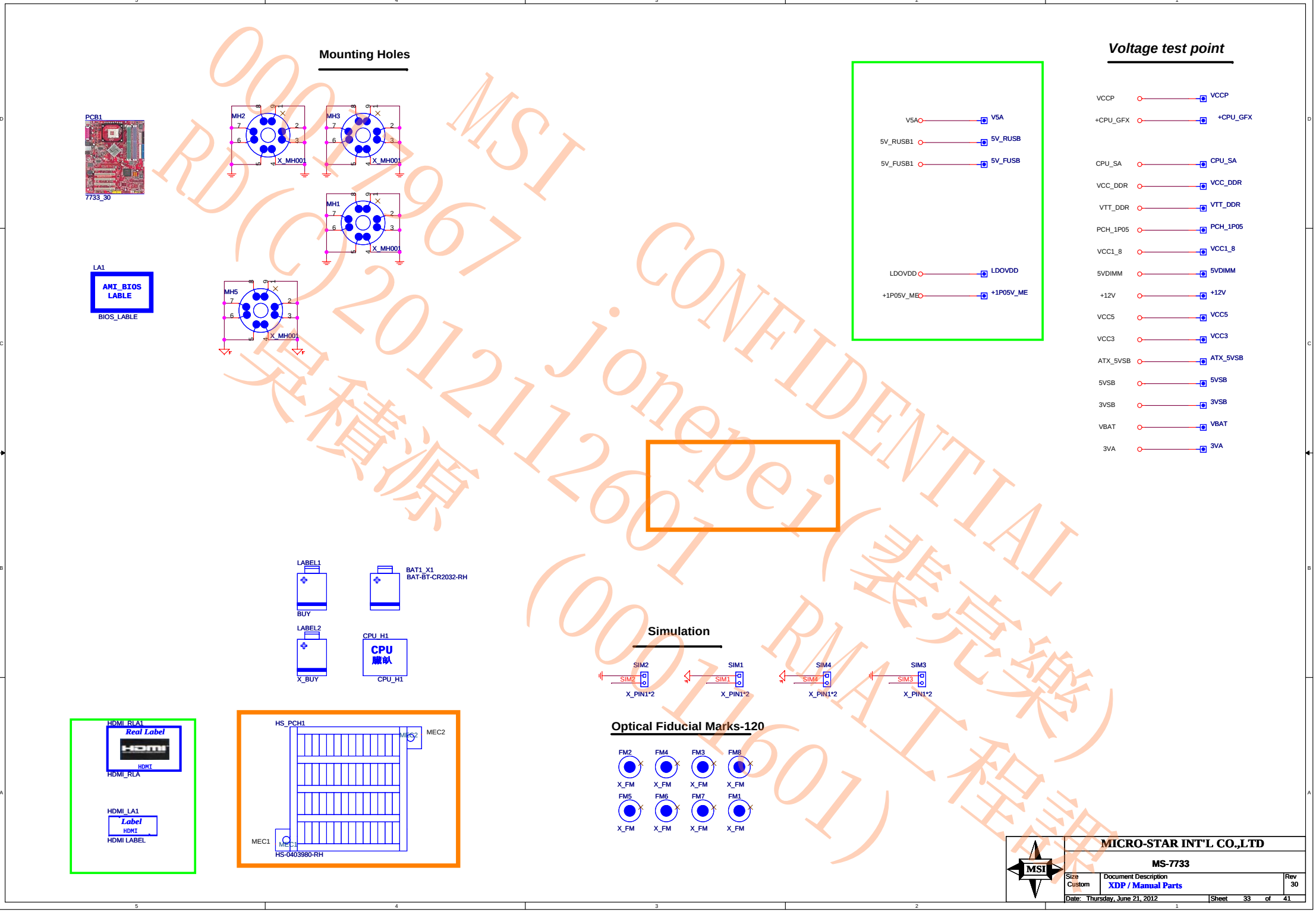

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EMI:cap. for signal return path

EMI

EMI

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